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Silicon nanocrystal photovoltaic device fabricated via photolithography and its current–voltage temperature dependence

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ABSTRACT

Photolithography is used as an alternative method to overcome the challenge of making anode and cathode contacts on a Si nanocrystal solar cell deposited on non-conductive substrates instead of reactive ion etching (RIE). The advantages of this method include better control of isolation mesa fabrication and the avoidance of device exposure to highly energetic particles which may cause unpredictable damage. The photovoltaic device fabricated shows an open-circuit voltage (V_{OC}) and a short-circuit current density (J_{SC}) of 270 mV and 0.124 mA/cm^2 respectively at room temperature under one-sun illumination. Current–voltage measurements were performed at temperatures (T) from 77 K to 300 K. A model that includes recombination-generation current in the depletion region is considered to explain the observed current behaviour of the device. An ideality factor very close to 2 was calculated based on Suns-V_{OC} measurement, which indicates that the device is limited by recombination in the depletion region. A discrepancy was observed between the peaks (1.47 eV) in the photoluminescence spectrum and maximum V_{OC} (0.81 V) extrapolated from the V_{OC}–T relation at 0 K. This discrepancy has been attributed to the temperature dependence of the carrier lifetime in the depletion region characterized by an activation energy later defined in this article.

1. Introduction

A tandem solar cell structure made using materials with different bandgaps is an effective way to reduce thermalisation losses. Due to the effect of quantum confinement, wide bandgap low dimensional structures can be fabricated with current nano-fabrication techniques. It is therefore, in principle, possible to make a solar cell with tunable bandgaps using primarily Si [1]. In the standard fabrication technique used in this work, crystallisation of Si nanocrystals occurs at temperatures $>1000\ ^{\circ}C$, narrowing the range of candidates that could be used as conductive substrates. As reliable conductive substrates for Si nanocrystal (NC) material are still under investigation, finding a substrate to make low-resistivity ohmic contact on either n- and p-type layers remains challenging. To overcome this problem, a "mesa structure" is used where the anode and cathode contacts are made on the same side of the device [2]. Reactive ion etching (RIE) is then required for the fabrication process to make these mesas on p–i–n Si nanocrystal thin films. However, RIE is likely to have a negative impact on device performance as the p–n junction is directly exposed to highly energetic particles. The p–n junction is a crucial part of a solar cell and even minor damage on the edge of this junction can cause significant degradation in its performance [3]. In addition, the etching rate is not easy to control as the Si-NC material is embedded in an oxide or nitride matrix which may have a very different etch rate compared to the Si-NC. The rate difference can cause a significant level of surface roughness on the thin-film material. In this work, an alternative method of fabrication avoiding the use of RIE is introduced. Instead of RIE, photolithography was applied to facilitate the making of mesas on the thin films. The p-type thin film was deposited first by reactive ion sputtering on a quartz substrate. We will call this layer the "bottom layer" of the device throughout this article. Photolithography was then employed to define mesas on the top of this bottom layer. Openings in photoresist were made to expose areas intended to become diodes. The rest of the area, still covered by the photoresist, allows contacts to be placed on the bottom layer. Intrinsic and n-type materials were then deposited to cover the surface of the mesa. A subsequent lift-off defined the i–n active areas. In spite of more fabrication steps in the photolithography method, they are comparatively more controllable and less likely

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to cause rough thin-film surface. Afterwards, annealing of the Si-NC material was followed by metallization and contact sintering to fabricate a working device. Suns-V_{OC} was employed to determine the ideality factor of the device. Current–Voltage relations at temperatures from 77 K to 300 K with and without illumination were obtained. Discussion of the *I–V* characteristics and bandgap analysis will follow. This work points out that the electrical performance of the Si nanocrystal solar cell may be limited by Shockley–Read–Hall recombination in its depletion region. Further improvement of similar devices should focus on reducing trapping states in the depletion region.

2. Material and methods

The thin-film material used in this work was deposited via RF sputtering onto quartz substrates in an argon atmosphere at a pressure of 1.5×10^{-3} Torr using a computer controlled AJA ATC-2200 sputtering system. 4-inch Si and SiO_2 targets and a 2-inch boron target were used for Si rich oxide (SRO) and dielectric deposition and for doping respectively. Before sputtering, the chamber was evacuated to a base pressure of at least 3×10^{-7} Torr. These sputtered thin-films on quartz substrates contained alternating layers of SRO and silicon dioxide (SiO_2). The thickness of each SiO_2 and SRO layer was 1.8 nm and 4 nm respectively.

The "unit-structure" made of a SRO layer and a SiO_2 layer with the former layer deposited on top of the latter will be addressed as a "bi-layer". The volume ratio of Si in the SRO layer, expressed as a percentage, is defined as the ratio between the deposition rate (nm/min) of Si and the sum of the deposition rate of Si and SiO_2. The deposition rate was calculated based on the thickness of either SiO_2 or SRO layer deposited over a certain time period measured with a Woollam VASE FQ-TH100 ellipsometer. The thickness determined with this method was verified by comparing to the value determined using X-ray reflectivity. The discrepancy between the two methods was $\pm 4.2\%$. The co-sputtered samples reported in this work had volume ratios at 55%, 60% and 66% by adjusting the sputtering power of the Si target while keeping the power for the SiO_2 target fixed. SRO layers were doped with B during sputtering where the boron RF power source was set to supply 34 W power to the sputtering gun. The number of bilayers deposited was 30. A 20 nm capping layer made of SiO_2 was deposited on the surface of each sample as a protective layer. After the deposition, the samples were annealed in a N_2-purged tube furnace at 1100 °C for 1 h to facilitate Si QD nucleation and growth.

After these B-doped alternating SRO/SiO_2 thin-films had been annealed, negative photoresist nLOF2020 was employed to define mesas on the film. The nLOF2020 photoresist was spun at a speed of 3000 rpm for 30 s and then prebaked at 110 °C for 1 min. The resist was then exposed for 4 s using a Quintel 6000 mask aligner equipped with an UV light source (365 nm) with a measured 10 mW/cm^2 intensity. The resist was post baked at 110 °C for 1 min and subsequently submerged in AS826MIF developer for 65 s to fully remove the unexposed photoresist. At this stage, the mesa areas on the thin-films could be clearly observed (Fig. 1a). These openings as shown in Fig. 1a became windows for subsequent SiO_2/SRO bilayer deposition. To remove undesired photoresist residue and other possible organic contaminants, the samples were cleaned in a Denton O_2 plasma asher at an O_2 pressure of 340 mTorr for 20 min. To further remove possible residue on the B-doped thin-films and hence to expose the underlying B-doped bilayer, the protective oxide capping layer was removed by hydrofluoric acid immediately before loading into the load lock of the sputtering tool. Undoped and phosphine-doped SRO/SiO_2 materials were then deposited following a similar sputtering process. A combination of Ar and PH_3 (99:1) was injected into the sputtering chamber at a flow rate at 3 sccm during PH_3-doped-SRO/SiO_2 material deposition.

When the second AJA deposition was finished, the nLOF2020 photoresist was removed using N-Methyl-2-Pyrrolidone (NMP) to define the mesas by liftoff (Fig. 1b). Then the SRO thin film was annealed at 1100 °C for 1 h again to achieve the Si nanocrystal formation in the undoped and PH_3-doped thin-films. Metal contact deposition was also achieved via a liftoff process on both the n and p-type Si NC thin film contact areas by using positive photoresist AZ6612. A mask designed to make openings on both bottom and top (undoped followed by PH_3-doped-bilayered thin films) layers was used during UV exposure. In the metallization process, similar to the previous SRO deposition, the aluminium contacts were defined via lift-off to complete the full structure of a photovoltaic device (Fig. 1c).

The thin-film materials investigated had 55%, 60% and 66% Si by volume (Si:SRO). Apart from this difference they shared a similar structure—30 B-doped bilayers, followed by 10 undoped bilayers and 30 PH_3-doped bilayers. Each bilayer is made of 1.8 nm SiO_2 and 4 nm SRO. SiO_2 layers were not doped during sputtering. Metal contacts were deposited on the top of B-doped thin-films and PH_3-doped thin-films respectively to make the devices available for electrical measurement.

3. Results and discussion

3.1. Current–voltage relation

The photovoltaic device with Si volume ratio of 66% in the SRO layers showed an open circuit voltage (V_{OC}) of 270 meV and a short circuit current density (J_{SC}) of 0.124 mA/cm^2 at 25 °C under 1-sun illumination. The current density is calculated based on the area of the mesa (overlapping region of p- and i-type bilayers). The Fill Factor of this device is 0.277. In contrast, *I–V* measurements on devices prepared with SRO volume ratios of 60% and 55% were not measurable. It is suspected that the comparatively low Si content leads to a very high resistivity which impedes the flow of current to such an extent that it is not measurable. An optimised Si percentage for photovoltaic purpose should be found for future fabrication of Si NC solar cells. The average size depends greatly on the stoichiometry of the SiO_X as pointed out by reference [4]. When the Si content is increased, the average size of Si NCs will generally be larger. According to the effective mass theory [5], the effective bandgap of the material will hence become lower. To ensure the effect of quantum confinement to a certain extent, a sufficiently low Si content in the device should be chosen. The Fill Factor and efficiency of the device are low probably due to the high resistivity and low V_{OC}. Therefore the primary challenge of such devices may be to improve the V_{OC}. According to our current results, the optimal ratio might be higher than 60% and could be around 66%. Both "illuminated" and "dark" *I–V* curves are shown in Fig. 2.

Transmission line measurements (TLM) showed a linear current–voltage relation between contacts both on the top and the bottom layers. The sheet resistance was measured at different temperatures using the circular transmission line method (CTLM). At 300 K, the sheet resistance of the bottom layer was $3.03 \times 10^7\ \Omega/sq$ ($\pm 1.77\%$), while the sheet resistance measured on the top layer of the device was $7.65 \times 10^5\ \Omega/sq$ ($\pm 1.74\%$). Here we used a method introduced in the literature to calculate the external series resistance of the device based on the mesa's geometry defined in Ref. [2]. It is defined as an external resistance because it does not include the resistance due to internal effects