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Effect of band mismatch on minority carrier transport in heterojunction solar cells

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ABSTRACT

By using transient-capacitance techniques we probe the mechanism of hole transport in amorphous/crystalline silicon heterojunction solar cells. The devices are formed by depositing undoped amorphous silicon followed by p-type amorphous silicon on n-type crystalline silicon wafers. The capacitance transients indicate that hole transport from p-type amorphous silicon to n-type crystalline silicon is hindered by hole accumulation in the depletion region of the crystalline silicon. The results are explained with a model based on electrostatic repulsion owing to hole build-up at the crystalline/amorphous interface. We apply these results to other heterojunction solar cells.

1. Introduction

Heterojuncion solar cells, HSC, are getting increasing attention as a viable photovoltaic technology. Minority carrier collection can be a serious problem in HSC depending on the band mismatch. The amorphous/crystalline silicon-heterojunction, (SHJ) is a good example of extreme mismatch. The chief advantage of this type of cell is that the front junction and backsurface field junction to the crystalline silicon (c-Si) are formed from hydrogenated amorphous silicon (a-Si:H) using low temperature processing that allows sharp interfaces. A further advantage is that little light is absorbed in the junction region because of the wider bandgap of a-Si:H (1.7 eV) than the c-Si (1.1 eV). The efficiency is high, as demonstrated by double-heterojunction "HIT" solar cells [1]. However, this advantage can be offset by difficulties in minority carrier collection because the band mismatch between amorphous and crystalline silicon produces a potential step that hinders charge collection. Photoemission measurements place the band discontinuity at the valence band with the most recent value being about 0.45 eV [2]. This value gives a small step at the conduction band which produces little problem for electron collection for a p-type c-Si base, but a more serious problem for n-type c-Si base or absorber.

Fig. 1, showing the junction region, illustrates this problem for n-type bases. The back surface field and metal contact as well as the transparent conducting-oxide contact to the p layer are omitted to emphasize the junction region. This figure is the result of a numerical solution of the Poisson equation at 300 K. The c-Si contains $3\times10^{15}\,cm^{-3}$ donors and $1\times10^{12}\,cm^{-3}$ acceptors, the *i* layer $1\times10^{16}\,cm^{-3}$ dangling bond defects, and the p layer $1\times10^{20}\,cm^{-3}$ acceptor dopants. The c-Si bandgap is 1.1 eV and the a-Si:H bandgap is 1.7 eV. The valenceband offset is 0.45 eV. The Fermi level in the c-Si was determined using Fermi statistics and in the p layer using the experimental relation between doping and conductivity activation energy [3]. The c-Si/a-Si junction is located at 2000 nm.

The figure clearly shows the difficulty for hole collection under illumination. A hole in the c-Si valence band must either surmount the large potential step to the a-Si:H transport level in the band tails [4] or tunnel directly or via defects through the i layer to be collected in the p layer. Recent measurements show that hopping conduction through defects in the a-Si:H i layer is faster than thermal emission over the barrier presented by the c-Si/a-Si:H band mismatch, even at the temperature of solar cell operation [5]. Since a-Si:H contains a large density of defects stretching from band to band, this result is not so surprising.

The process is different for holes moving from the a-Si:H p layer to the c-Si n layer. Holes leave the p layer and enter the i layer at the transport level just above the valence band. Thus we expect that hole transport through the i layer will be faster than for the case where holes enter the i layer from the n layer far above the band tails. Therefore we might expect that, for example, transient capacitance measurements of hole motion in the two directions to be quite different with the time for holes moving toward the c-Si to be shorter than in the opposite direction. Once the hole traverses the i layer it enters the c-Si below the valence band and is confined by the valence band near the interface producing a large density of holes. Fig. 1 shows holes concentrated at the interface at equilibrium. The majority of these holes are confined within 1 nm of the interface.

In this manuscript we explore hole transport from the p layer to the n layer. We accomplish this by using capacitance to measure holes as a function of time following a bias change designed to remove holes from the c-Si region near the interface. The resulting

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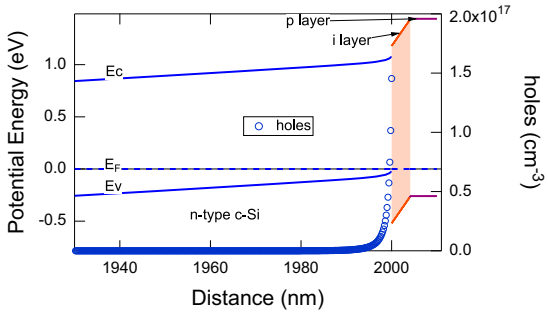

Fig. 1. Electron energy diagram for the heterointerface region of a SHJ cell with n-type base at equilibrium. The front and back regions are omitted for clarity. The conduction and valence bands are labeled by E_C and E_V, respectively. The Fermi level is E_F. The circles represent the hole density.

capacitance transients are of much different character from those of holes moving from c-Si to a-Si:H [5]. The data suggest that the Coulomb potential owing to the build up of the holes at the c-Si interfacial region determines the transients.

2. Material and methods

2.1. Samples

For the measurements, we use samples describe in Refs. [5,6]. All are SHJ solar cell devices fabricated using hot-wire chemical vapor deposition on high-lifetime n-type, 1.6-Ω cm, Czochralski wafers. Details can be found in Ref. [6] The amorphoussilicon i layer thickness at the front emitter varies from 3.2 nm to 16 nm. The 20 nm thick boron doped p layer is the same for all i layer thicknesses.

2.2. Measurement

Capacitance transient techniques are non-equilibrium measurements that detect recovery of charge imbalance owing to disturbances from equilibrium. They are well suited to probe hole motion from p-type a-Si:H to c-Si. The junction-capacitance method uses a lock-in amplifier (Stanford Research Systems Model SR850) at a frequency of 100 kHz and an ac test voltage of 0.03 V rms. The sample is placed in a heated holder capable of maintaining a stable temperature ($\pm$ 0.1 K) between 100 K and 600 K. Data are collected at a rate of 50,000 samples/s. Digital signal averaging and data storage only at logarithmic time intervals reduce the data set to a manageable size. For some capacitance transient measurements, we use a SULA deep-level transient-spectroscopy system.

Hole motion toward the p layer is probed using a short light flash or forward bias pulse and measuring the resultant capacitance transient [5]. The transients are fitted with stretched exponentials with the stretching parameter near unity. To probe hole motion away from the p layer we use the following procedure:

- The device is cooled to the measuring temperature and the bias is set to 0 V or a small forward bias and the capacitance (C) is measured.
- A reverse bias pulse removes holes and electrons from the c-Si depletion region (see Fig. 1).
- Following the end of the pulse, the capacitance returns to its original value as electron and hole motion reestablishes equilibrium. Because of their much higher mobility, electrons rapidly flow from the contact into the c-Si establishing the original depletion region. This process is too fast to be observed by our capacitance technique. Thus the capacitance transient represents hole migration through the i layer into the c-Si finally saturating when the original interfacial hole population is reestablished.

3. Results and discussion

The circles in Fig. 2 show the recovery of capacitance, represented by $\Delta C/C$, following a reverse bias pulse to -4 V for 1 s. This bias removes most of the holes that are originally in the c-Si depletion region (see Fig. 1). $\Delta C/C$ is the relative change in capacitance from its final value at long time normalized to the final value. Because of the rapid electron motion, the increase in $\Delta C/C$ represents only holes that are returning into the c-Si depletion region. The dashed line in Fig. 2 represents motion from c-Si into a-Si:H. Here the excess holes are produced by light absorbed in the c-Si n layer. This type of experiment was used to explore hole collection in a series of these heterojunctions [5]. Note the different shape of the two transients.

Holes returning to the depletion region produce a the slow, logarithmic (straight line region) rather than the exponential transient resulting from hole motion from c-Si into a-Si:H. The solid curve in the figure is a fit of a stretched exponential with a stretching parameter=0.95 to this type of data. We find this general behavior for all samples. The main difference among samples is that the time to return all the holes to the depletion region (saturation) increases with i layer thickness.

It is surprising that nearly 0.1 s is required to reach steady state when all holes have returned to the depletion region since transport through the i layer at the transport level should be sub-microsecond. This behavior suggests that the ability of holes to enter the c-Si depletion region is hindered. A possible mechanism that would slow down holes entering the depletion region would be the repulsive potential they produce. Such an effect has been observed to affect the dynamics of charge trapping by defects in a variety of semiconductors [7–10]. In our case the "trap" is the narrow region at the c-Si/a-Si:H interface. As holes collect in this region they steepen the potential resulting in confinement at the interface. In a sense these are "self trapped" holes since c-Si does not contain enough defects to accommodate these holes. Fig. 1 shows the large hole density at the interface.

To explore this idea, we perform the type of experiment used to measure charge trapping in defects [7,10]. In this experiment the sample is held at far reverse bias to remove holes from the depletion region and C measured. Then a short forward-bias voltage-pulse injects holes into the depletion region. At the end of the voltage pulse, the capacitance returns to its initial value as the injected holes leave the depletion region. The peak amplitude of the transient, $\Delta C(t=0)$, measures the number of holes injected during the bias pulse. This experiment is repeated with increasing pulse times (t_p) until reaching steady state with holes leaving the

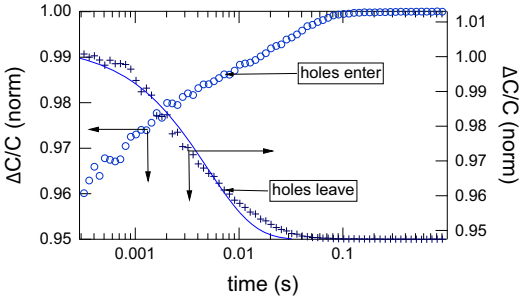

Fig. 2. The circles represent a normalized capacitance change following a -4 V bias pulse for 1 s. Sample is held at 155 K and 0.3 V. The end of the reverse bias determines the zero of time. The + symbols represent a normalized capacitance change following a light flash. Sample is held at 0 bias and 154 K. Sample has a 12 nm thick *i* layer.