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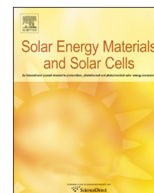

Conversion efficiency and process stability improvement of electron beam crystallized thin film silicon solar cells on glass

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ABSTRACT

Liquid phase crystallization (LPC) using e-beam or CW-laser line sources of amorphous or nanocrystalline silicon films has emerged as new method to form high quality absorbers on cheap substrates. A disadvantage of electron beam crystallization was the necessity to use amorphous SiC_x layers in contact with the silicon to maintain a stable crystallization process, resulting in high surface recombination. In this work we investigate capping layers to enable e-beam induced LPC on alternative interlayer materials especially SiO_2 and characterize the morphological and electrical properties of these layer stacks. Photoluminescence measurements of LPC absorbers on SiO_2 layers exhibit significantly increased radiative recombination compared to SiC_x. Fabricated hetero-junction cells achieved a new emitter area efficiency record for electron beam induced LPC solar cells of 9% using the FrontERA contact system and H passivation.

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1. Introduction

Polycrystalline silicon thin-films directly grown on cheap substrates are very attractive for photovoltaic applications due to the high electronic quality, long-term stability and kerfless fabrication [1–3]. The major obstacle to realize highly efficient polysilicon thin-film solar cells is the formation of a high quality absorber on glass, due to its limited thermal stability. For the common solid phase crystallization (SPC) approach an efficiency record of 10.4% was demonstrated [4]. However, the limiting factor is the open circuit voltage (V_{oc}) [5] which is usually below 500 mV on glass, imposed by intra-grain defects present at level of 10^{16} cm^{-3} [6]. A considerable reduction of intra-grain defect concentration and thus a boost in open circuit voltage well above the SPC limit were achieved by liquid phase crystallization (LPC), using line sources such as electron beam [7,8] or CW diode lasers [9]. LPC forms coarse grained absorbers with grains up to centimetres in length and millimetres in width, exhibiting an intra-grain defect density up to 2 orders of magnitude below SPC material [6]. A critical component in this approach is the interlayer between substrate and silicon absorber as this layer has to fulfill different tasks. Depending on the device concept it has to provide absorber doping and/or optical confinement, but more important is the wetting behaviour and the level of surface passivation to minimize carrier recombination at this interface. Best device results on electron beam crystallized absorbers were achieved using a combined stack of SiC_x as wetting promoter and SiO_2 diffusion barrier [8,7]. The excellent wetting properties of SiC_x enabled a stable crystallization process but surface recombination velocity was found to exceed $S_{SiC_{x/Si}} = 10^6$ $cm\,s^{-1}$ [10]. In this study, we present a method to achieve improved process stability and homogeneity for LPC processes using comparatively inhomogeneous line sources by adding an additional protection layer on top of the absorber. It is known from the literature that the wetting of silicon is enhanced by capping layers [11,12] with adequate thermal stability. However, this technique was applied on high temperature stable substrates for very slow scanning speeds which are in contrast to LPC on glass. Beside the enhancement of process stability this layer acts as protection layer against impurity diffusion from surrounding environment during the process or during device fabrication.

2. Sample preparation

All samples were prepared on Corning Eagle XG glass substrates with 1.1 mm thickness. The substrates were cleaned using a commercial alkaline cleaning agent at elevated temperatures in an ultrasonic bath. After drying the samples with nitrogen, a diffusion barrier of 200 nm SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) using silane (SiH_4) and nitrous oxide (N_2O). Silicon carbide layers were deposited on reference samples by RF magnetron sputtering from a microcrystalline SiC target at a thickness of 20 nm. The 10 μm thick silicon absorber was deposited using high-rate electron beam evaporation [13] at 600 °C and a rate of 300 nm · min^{-1}. Prior to crystallization, the

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samples were heated at 650 °C for several minutes to reduce thermal stress during crystallization. Afterwards crystallization was performed using a line shaped electron beam at a constant scanning speed of 6 mm s^{-1} (details [8]). In order to prevent silicon dewetting on single SiO_2 layers, an additional reactively sputtered SiO_2–capping layer was deposited before crystallization. After crystallization, the capping layer was removed by diluted HF. a-Si:H/c-Si hetero-junction solar cells were fabricated using the contact system described in [7].

3. Results

3.1. Absorber morphology

Fig. 1 shows an electron backscatter diffraction (EBSD) map of the crystallized absorber. The electron beam was scanned during crystallization from left to right. Hence the image shows the beginning of the grain formation on the left followed by the stationary crystallization process on the right. The change in morphology can be explained by the fact that at the leftmost point the temperature (preheat temperature) is too low in order to melt the silicon completely. The molten part of the silicon nucleates at the liquid:solid interface and causes the grains to grow perpendicular to scanning direction. A detailed description on the evolution of the morphology can be found in [14]. After a short period of time, the beam has introduced a sufficient amount of heat to melt the silicon completely. At this threshold, the crystal growth occurs in scanning direction with the solidificated regions acting as seed.

As it can be seen from the EBSD map, the crystallization process forms extended grains in scanning direction. Using wet chemical texturing, the grain size was determined to exceed several cm in scanning direction for both SiC_x and SiO_2 interlayers (not shown here).

3.2. Influence of capping layers

To study the influence of capping layers on the process stability, we deposited silicon dioxide layers of different thicknesses on top of the silicon absorber and determined the process window in terms of energy limits during crystallization (Fig. 2).

The graphs were obtained by subsequently increasing the energy during a single scan of the e-beam over the sample for different capping layer thicknesses. In region (I) columnar grains about 10–20 μm in size are grown during crystallization. The black curve represents the threshold energy necessary to obtain a morphology characterized by longitudinal grains (region (II)) entirely through the absorber thickness. We normalized the applied energy to this value. The upper, grey curve denotes the maximum tolerable energy. A further increase in energy will cause the layers to delaminate (region (III)). According to Fig. 2, a 200 nm thick capping layer allows a 17% higher energy than the crystallization threshold without dewetting, which is about the same value if uncapped silicon is crystallized on SiC_x. A capping layer of 50 nm is not sufficient as the threshold for longitudinal grains and the delamination limit is within the homogeneity range of our electron beam system. The crystallized silicon in regions I and II were characterized using Raman spectroscopy. Fig. 3 illustrates the full width half maximum (FWHM) of the c-Si phonon mode as well as the peak position with respect to the applied energy, to characterize the film in terms of microstrucure and stress. A clear correlation between applied energy density and reduction of stress and FWHM was found only for region I. As soon as the threshold energy limit is passed, a saturation is observed for both FWHM and peak position. The FWHM in this region is close to a c-Si reference (CZ-wafer) with a minimal amount of built-in stress.

By comparing the results obtained by Raman-spectroscopy with the EBSD data in Fig. 1, this can be explained by the increase in crystal size with increasing melting depth for energies below the linear grain region. In addition, a higher amount of heat is present at the interlayer causing the glass to soften and thus to release film stress. Once linear grains are formed, the stress is relaxed completely as no solid silicon phase at the interlayer exists.

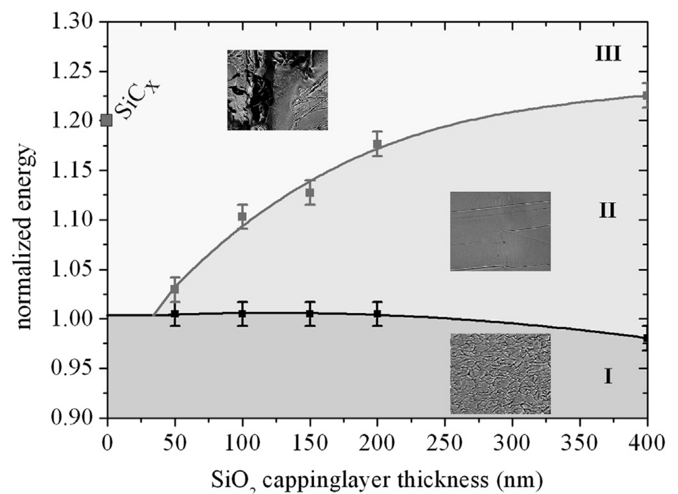

Fig. 2. Threshold energy to form longitudinal grains and delamination limit vs. capping layer thickness and optical micrographs of the resulting morphology (inset).

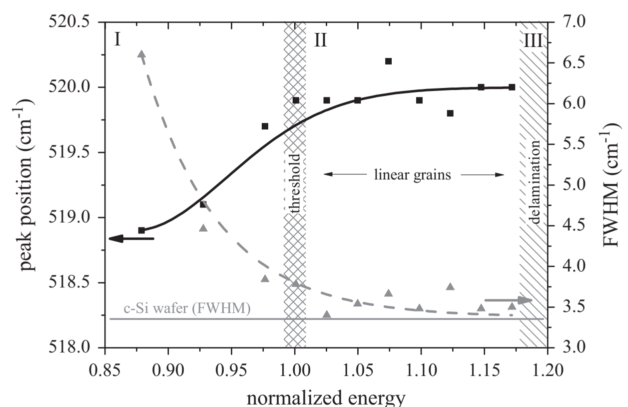

Fig. 3. Film stress and microstructure determined by Raman spectroscopy as a function of applied energy density (200 nm capping layer thickness).

Fig. 1. EBSD image of an electron beam crystallized absorber on glass.

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