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First quadrant phototransistor behavior in $CuInSe_2$ photovoltaics

A. Rockett [a,*], J.K.J. van Duren [b], A. Pudov [c], W.N. Shafarman [d]

[a] Department of Materials Science and Engineering, University of Illinois, 1304W. Green St., Urbana, IL 61801, USA
[b] Intermolecular Inc., 3011 North First Street, San Jose, CA 95134, USA
[c] Solexant Inc., 2385 Bering Dr., San Jose, CA 95131, USA
[d] Institute of Energy Conversion, University of Delaware, Newark, DE 19716, USA

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ABSTRACT

Temperature-dependent current voltage measurements on a $CuInSe_2$ (CIS) solar cell are described and analyzed in detail. At relatively low temperatures, the device is shown to exhibit operation as a phototransistor, evidenced by light flux dependent current in the first quadrant of the current/voltage curve prior to the onset of a high differential resistance region of the curve. The phototransistor behavior is not restricted to light with short wavelengths (such as would stimulate the front contact materials—CdS and ZnO), and has a similar sensitivity to light over a wide range of intensities. Other aspects of the device operation are analyzed including observation of a photoconductive shunt and series differential resistance component, neither of which requires short wavelength light to be observable, a non-light-sensitive diode reverse-saturation current, and characterization of the back diode in the device. It is argued that the presence of an effective back diode also requires a bias voltage to develop across that diode under a variety of operating conditions that could reduce the open circuit voltage of the device. The potential for characterization of minority carrier properties in the device absorber layer through further controlled study of phototransistor behavior in the devices is noted.

1. Introduction

Photovoltaic devices based on $CuInSe_2$ (CIS) and other chalcopyrites have demonstrated the highest efficiency of any thin-film, polycrystaline or amorphous device, [1] and approach the efficiency of single-crystal single-junction devices. However, CIS devices fall short of the Shockley–Queisser efficiency limit [2]. Further optimization of the champion cells will require a more detailed understanding of their operation. Likewise, production of the devices can be highly sensitive to process conditions and in particular to reactions at interfaces, whether a given interface produces an ohmic or Schottky type junction, and how charge is transported both within the absorber layer of the device and at the contacts and surrounding junctions.

The behavior of CIS solar cells has been studied extensively and many groups have observed a sudden increase in series differential resistance in some devices under light exposure when biased above the open circuit voltage (V_{oc}). In other words, into the first quadrant of the current–voltage plot. [Note that we use the term differential resistance to refer to the resistance of a component of the device equivalent circuit such as the back contact junction. In the case of diode-like behaviors this differential resistance changes exponentially with the bias voltage across that diode.] This first-quadrant "roll-over" has been explained as the result of a Schottky barrier at the back contact [3]. Other data in which the sudden increase in differential resistance only occurs under illumination when the light is filtered to provide wavelengths under 600 nm (often referred to as the "red kink effect") was proposed to result from defects in the CdS layer at the front of the device [4]. Back contact effects have also been studied in CdS/CdTe solar cells, in which the effects are often more pronounced, and the results were described as due to the electron current in the base (CdTe) layer reaching the back contact and recombining there [5]. The explanation given in that CdTe work includes the observation that for a reverse-biased back contact the current in the first quadrant saturates at a level related to the reverse saturation current in the back diode.

This work presents a somewhat similar analysis of a CIS-based solar cell and gives an interpretation of a low differential resistance region in the first quadrant of the current/voltage curves. The basic physics of the phenomenon described here is similar to that of Niemegeers [5]—electron transport through the base—although in this work the limiting current is much greater—a significant fraction of the photocurrent. In addition to the back-diode current saturation behavior itself, the studied device shows the reverse breakdown of that back diode (we presume that it is a highly defective back diode); this breakdown reduces the contact differential resistance at higher voltage and temperature.

* Corresponding author. Tel.: +1 217 333 0417.
E-mail addresses: arockett@illinois.edu, arockett@uiuc.edu (A. Rockett).

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The behavior overall is consistent with the operation of a phototransistor and is interpreted in those terms. The most important result of such an interpretation is that devices produced and tested specifically to show such phototransistor behavior can provide a very effective method for testing the properties of minority carriers in an operating solar cell. Because the behavior described here is not often observed in CIGS devices it may be associated with unique features of the devices tested, which were produced at lower temperature than normal process conditions. We were unable to establish a clear connection between the deposition conditions and the phototransistor behavior, which is atypical in these devices. We presume that the behavior of this device was the result of the low temperature processing. The phototransistor behavior observed should be present in other devices if a significant back Schottky contact barrier is present and if photocarriers are collected by this back junction under forward bias (in the first quadrant).

2. Experimental

Several photovoltaic devices were fabricated under different conditions at the University of Delaware's Institute of Energy Conversion (IEC). To keep this paper focused, only the behavior of one of those devices is described here, although the conclusions reached are consistent with the behavior of the other devices, some containing as high as 30% Ga, relative to In+Ga. The CIS absorber layer in this device was deposited at substrate temperature 480 °C, lower than typical depositions at 550–580 °C. Otherwise the device was fabricated following procedures described in detail elsewhere [3]. The device consisted of an ~2μm-thick single layer CIS absorber evaporated onto Mo-coated soda-lime glass at a substrate temperature of 480 °C. The Mo was 0.7 μm thick and was deposited by dc sputtering. Following CIS deposition, a heterojunction was formed with 40–50 nm of CdS deposited on the CIS by chemical bath deposition. A transparent TCO layer finished the device consisting of an ~50 nm thick high resistivity ZnO (~10 Ω cm) layer in contact with the CdS and a 150 nm thick low resistivity (In_2O_3)(SnO_2) [ITO] (25 Ω/□) layer as a top contact. The resulting device had a short circuit current density J_{sc}= 34.1 mA/cm^2, an open circuit voltage of 450 mV, and a fill factor of 69.5%, yielding an efficiency of 10.7% as measured at 25 °C at Nanosolar. Current/voltage measurements were performed over a broad range of temperatures from −175 to 65 °C in 20 °C increments. Illumination conditions were: (1) in the dark, (2) using white light from a solar simulator lamp (100 mW/cm^2) and the same light filtered (3) to block all wavelengths below 600 nm, (4) through a neutral density filter to attenuate the light uniformly across the spectrum to ~32 mW/cm^2 intensity, (5) through a neutral density filter to attenuate the light to 0.7 mW/cm^2, and the two neutral density filters each separately combined with the 600 nm filter [resulting in illumination conditions (6) and (7), respectively].

3. The device

In the discussion of results that follows it will be useful to refer to the equivalent circuit shown in Fig. 1. The device consists of several important regions that contribute to the observed behaviors. The heterojunction is formed between the CIS and CdS and includes a simple photoconductive series differential resistance due to the CIS layer (see discussion below).

The main junction extends from the heterointerface through the depletion region. In Fig. 1 this is shown to extend roughly one quarter of the way through the CIS or roughly 0.5 μm.

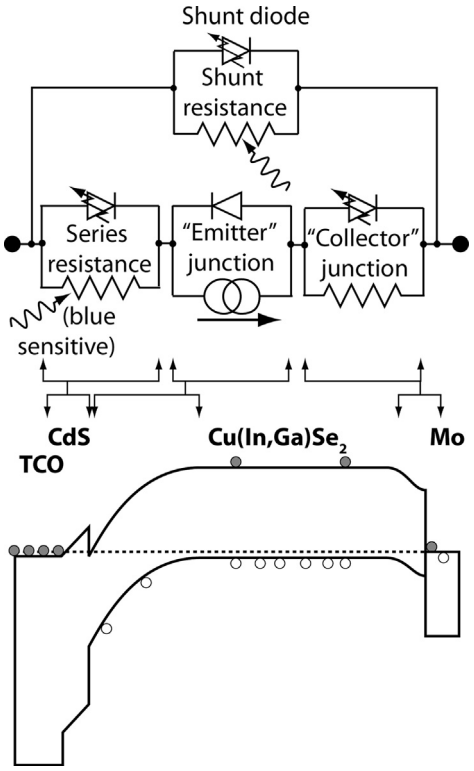

Fig. 1. shows the equivalent circuit of the device (top) and the corresponding equilibrium band edge diagram (bottom). The "lightning bolt" through the circuit symbols indicates that their contribution is light sensitive.

Observations made on similar devices (deposited at a higher temperature) using drive level capacitance profiling (DLCP) indicate a 0.5–0.9 μm depletion width depending upon illumination and temperature, consistent with numerical simulations of the devices tested here [6]. Finally it has been found that Mo typically produces a modest-height Schottky barrier with respect to CIS with a height value that is sensitive to the formation of $MoSe_2$ at the interface.[3,7,8] The measurements below show that the device studied here indeed has a Schottky barrier at the rear, as discussed in detail below.

We therefore expect that the complete device has two depletion regions, one near the heterojunction (here the "emitter") and one at the back contact (here the "collector"), resulting in a band edge diagram similar to an n-p-n transistor (Fig. 1) with the CIS providing the p-type "base" region. If the diode-like back contact contributes a significant differential resistance the device can be expected to operate as a transistor. As with any bipolar transistor the recombination current in the base (the CIS) must be removed by an external contact to avoid charge buildup and shutdown of the transistor. In a phototransistor, this charge is removed through photogeneration of electrons in the base, which then escape to the emitter or the collector. Thus the photocurrent acts as base current and can turn the transistor on.

When the device is passing current in the positive direction, minority carriers are injected into the base due to a positive voltage that develops across the emitter–base junction under light or forward bias. If the collector junction differential resistance is low enough, the injected emitter current/voltage relationship controls the diode differential resistance. However, at low temperature, the collector junction may dominate the device differential resistance under conditions of strong emitter injection (forward bias). When the device is passing current in the reverse direction the collector junction is forward biased and only reverse