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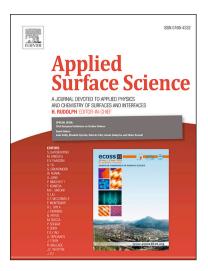
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ACCEPTED MANUSCRIPT

Formation of extended thermal etch pits on annealed Ge wafers

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An extended formation of faceted pit-like defects on Ge(001) and Ge(111) wafers was obtained by thermal cycles to T > 750 °C. This temperature range is relevant in many surface-preparation recipes of the Ge surface. The density of the defects depends on the temperature reached, the number of annealing cycles performed and correlates to the surface-energy stability of the specific crystal orientation. We propose that the pits were formed by preferential desorption from the strained regions around dislocation pile-ups. Indeed, the morphology of the pits was the same as that observed for preferential chemical etching of dislocations while the spatial distribution of the pits was clearly non-Poissonian in line with mutual interactions between the core dislocations.

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I. INTRODUCTION

Despite recent advances in the van der Waals epitaxy of two-dimensional semiconductors [1-7], bulk group-IV still plays a leading role in current complementary-metal-oxide-semiconductor (CMOS) technology. Within group IV, nonsilicon-oriented research is mainly devoted to Ge. SiGe heterostructures monolithically grown on Si are the ideal test bed for understanding alloying [8-11] and the interplay between elastic/plastic relaxation at the nanoscale [12-22] Their also being promising candidates for integrating optical communications into a CMOS platform, thanks to their optical properties potentially compatible with the C-band transmission window [23]. Ge wafers, on the other hand, are the substrates of choice for the epitaxial growth of high-efficiency multi-junction solar cells based on III-V semiconductors [24-29] and have also been shown to be suitable CMOS compatible templates for graphene overgrowth [30-32]. All these applications require a highly-demanding surface quality of the epi-ready Ge substrates. Indeed, any deviation from a perfect surface will be a nucleation point for a defect or a cause of a non-uniform epi-stack. In particular, one of the main issues affecting the manufacturing of semiconductor wafers is the formation of extended secondary defects such as crystal-originated pits (COPs) and L-pits (also referred to as A-Swirls) resulting from the aggregation of intrinsic point defects [33]. While COPs are voids produced by the aggregation of vacancies, it is generally assumed that the formation of L-pits is related to dislocation loops either intrinsically formed during the wafer manufacturing [34, 35] or by misfit strain in the case of SiGe heteroepitaxy [36]. Download English Version:

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