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Long-term stability of photodetectors based on graphene field-effect transistors encapsulated with Si_3N_4 layers

Fang Su[a,1], Zhaohao Zhang[b,1], Shasha Li[a], Peian Li[a], Tao Deng[a,*]

[a] School of Electronic and Information Engineering, Beijing Jiaotong University, Beijing 100044, China
[b] Key Laboratory of Microelectronics Devices & Integrated Technology, IC Advanced Process R&D Center, Institute of Microelectronics of Chinese Academy of Sciences (IMECAS), 100029 Beijing, China

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ABSTRACT

Graphene photodetectors have drawn a lot of interest due to their superior properties. For entering real applications, the existing open-face graphene photodetectors need to be properly protected to obtain long term stability. Here we demonstrate a facile method to obtain air-stable graphene photodetectors by directly depositing Si_3N_4 layer on the surface of buried-gate graphene field-effect transistors (GFETs). The electrical and photoelectrical properties of the Si_3N_4-encapsulated GFETs were carefully investigated and compared with that of the reference open-face GFETs. A photoresponsivity of 6.3 mA/W was obtained under a gate bias of 6 V, which was over 4 times higher than the photoresponsivities of typical back-gated GFET photodetectors under gate biases up to 80 V. Furthermore, the Si_3N_4-encapsulated GFET photodetectors demonstrated good stability for several months.

1. Introduction

Graphene is one of the most promising materials for high-performance photodetectors. The unique gapless bandstructure of graphene enables photodetection from ultraviolet to terahertz spectral regimes [1,2]. Besides, graphene demonstrates ultrafast carrier dynamics [3,4], wave-independent absorption [1,5,6], photocarrier multiplication [7–9] and tunable optical properties via electrostatic doping [10,11]. Most of the research work on graphene-based photodetectors fucuses on increasing the responsivity of the devices, accelerating their response speed and extending their operation wavelength range [12–16]. However, there are few reports about the long term stability and robustness of these devices, which are mandatory for practical applications. Open-face graphene devices are very sensitive to environmental factors such as H_2O, O_2 and impurity particles, which always cause unintentional p-type doping of graphene [17,18] and dramatic changes of electrical resistances [19]. Therefore, it is crucial to isolate graphene from the surrounding environment.

A simple method to improve the stability of graphene devices is to encapsulate them with a protective layer. There have been some reports on encapsulating graphene devices using titanium (Ti) [20], pentacene [21], amine based self-assembled monolayers [22], plasma-enhanced chemical vapor deposited (PECVD) grown Si_3N_4 [23–25], Al_2O_3 [26], and BN [19,27]. Compared with other materials, Si_3N_4 has some outstanding properties. Firstly, Si_3N_4 has ultra-low loss and broad transparency [28]. Secondly, Si_3N_4 offers efficient chemical protection over diverse gases and liquids, such as O_2, H_2O [25] even coffee [23], and robust mechanical protection against impacts [23]. Thirdly, Si_3N_4 can cause an effective n-type doping of graphene, improving the electric properties of graphene devices [20,24,25]. Last but not least, the Si_3N_4 depositing process is compatible with the conventional integrated circuit (IC) technology. Thus, Si_3N_4 is an ideal material to encapsulate and protect graphene photodetectors.

In this paper, a buried-gate GFET-based photodetector encapsulated with Si_3N_4 layers was demonstrated. The electric and photoelectrical properties of the GFETs before and after the Si_3N_4 depositing process were investigated and compared with each other. Furthermore, the long-term stability of the Si_3N_4-encapsulated GFETs was tested and compared with that of the reference open-face GFETs.

2. Experiments

The fabrication process of the graphene field effect transistors (GFETs) encapsulated with silicon nitride (Si_3N_4) layers is shown in Fig. 1. Firstly, a layer of Si_3N_4 with the thickness of 200 nm was deposited on a 500-μm-thick silicon wafer by plasma enhanced chemical

* Corresponding author.
E-mail address: dengtao@bjtu.edu.cn (T. Deng).
[1] These authors contributed equally.

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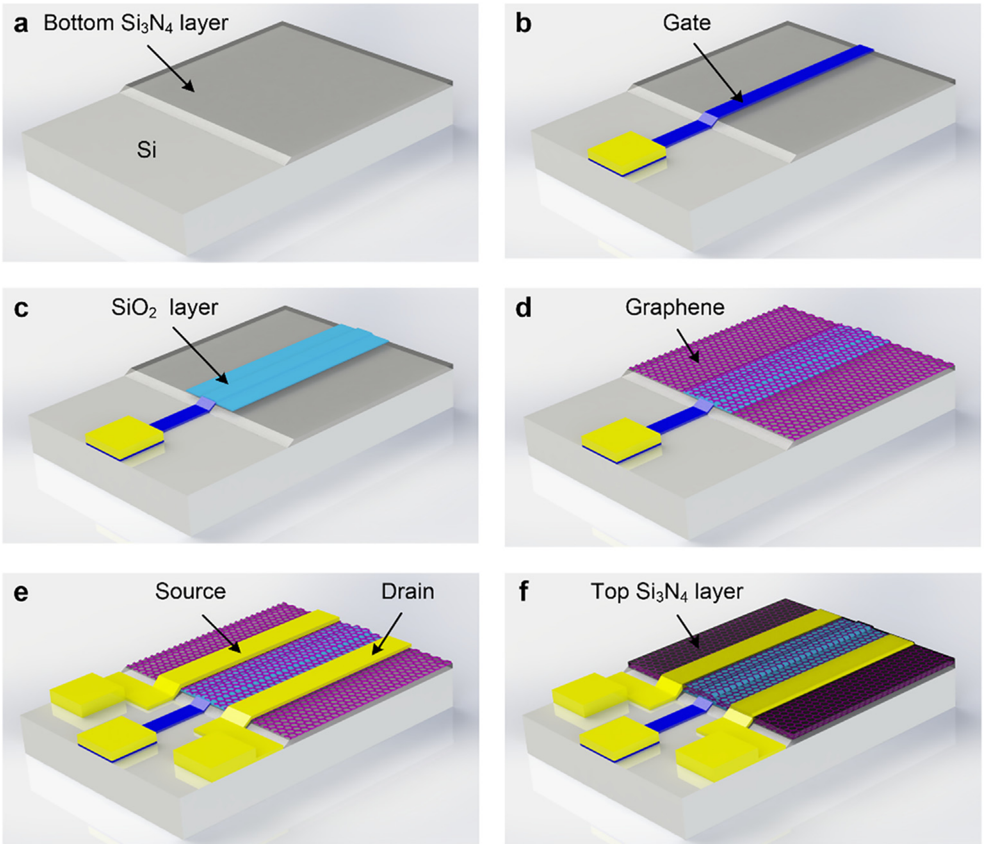

Fig. 1. Schematic of the process for the fabrication of GFETs encapsulated with Si_3N_4 protective layers. (a) Depositing the bottom Si_3N_4 protective layer. (b) Sputtering the buried Cr/Pt gate electrode. (c) Depositing the SiO_2 dielectric layer. (d) Transferring and patterning monolayer graphene. (e) Evaporating the Cr/Au source and drain electrodes. (f) Depositing the top Si_3N_4 protective layer.

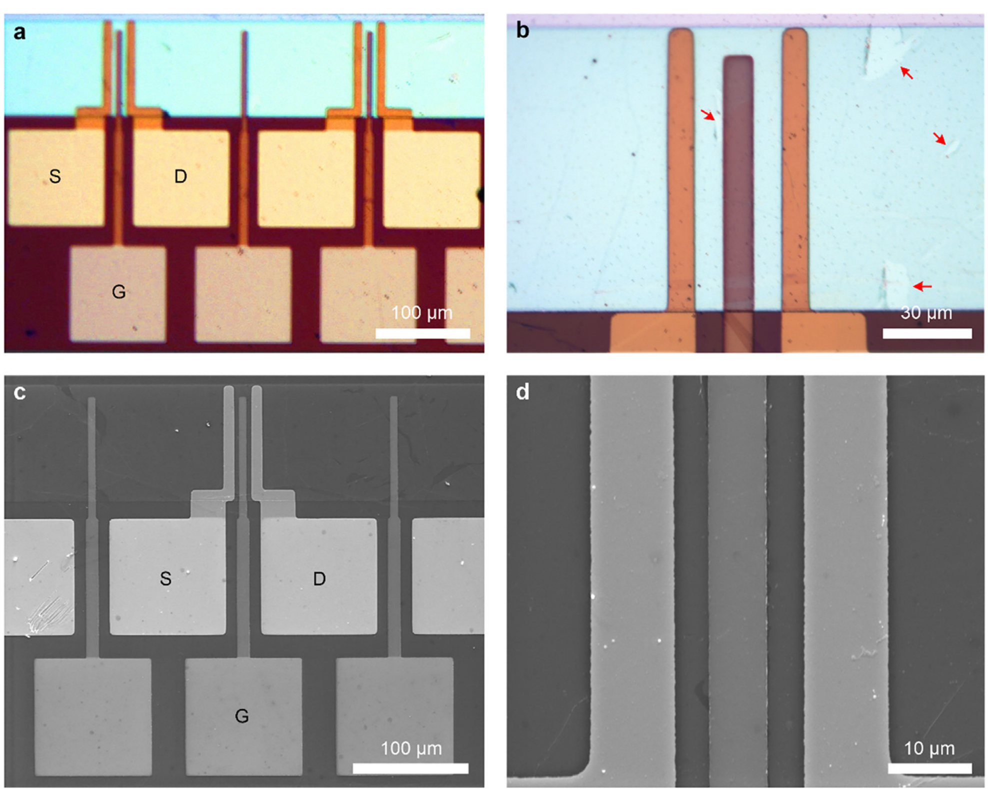

Fig. 2. Optical and SEM images of GFETs encapsulated with Si_3N_4 protective layers. (a) An optical micro image of the Si_3N_4-encapsulated GFETs and (b) the zoomed-in details of the graphene conductive channel. (c) A SEM image of the Si_3N_4-encapsulated GFETs and (d) the zoomed-in details of the graphene conductive channel.