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A joint thermal–electrical analysis of void formation effects on concentrator silicon solar cells solder layer

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ABSTRACT

It is known that the formation of voids in solar cell solder joints leads to a worsening of their heat sinking capabilities, causing an increase in the average device temperature and thermal resistance. This phenomenon can be detrimental for the solar cell's performance, since the open-circuit voltage linearly decreases with temperature. The performances of silicon solar cells, in the presence of voids in the cell solder joint, are studied by means of numerical simulations and of an analytical thermal model which can assess the local temperature increase at cell surface due to a single isolated void in the solder joint. The results show that for small isolated voids the analytical model gives temperature peaks above the voids which match very well with the simulations result, within 5% of relative error. The analytical model also gives an estimation of the whole device thermal resistance, in the presence of a regular pattern of non-interacting voids all with the same surface area. For a 10×7 pattern of small area voids the analytical value for the device thermal resistance matches well with the results of numerical simulations, with a maximum error of 17.3% at 70% void coverage. To determine the temperature profile of the device surface we have implemented a thermal finite element analysis (FEA) which employs a detailed 3D model of the real morphology of voids in the solar cell, obtained by X-ray inspection. The resulting temperature map has been used as an input parameter for the subsequent electrical simulations performed by means of PSPICE software, which is based on a distributed 2.5 D electrical model of the solar cell. Results show that, for a concentrating factor of $100\times$, a real void pattern with 36.6% void coverage does not noticeably affect the performances of a concentrator silicon solar cell.

1. Introduction

Soldering processes in large area semiconductor devices are often affected by the formation of voids at the interface between device and substrate. Void formation may be due to a bad soldering process, or arise as a result of thermo-mechanical stresses introduced during device operations [1–3]. These voids have a deleterious effect on the heat sinking capabilities of the device [4,5] since they are responsible for a local increase in thermal resistance. This, in turn, can drive the formation of further voids and compromise the reliability of the device.

Concentrating photovoltaic cells are wide area devices that periodically undergo large thermal flow variations. In that, an assessment of the impact of void presence on solar cell temperature distribution and performances can be very useful.

In this work, four concentrator silicon solar cells manufactured by Narec Solar, Blyth, UK (with an area of 19 mm × 14 mm each) have been soldered to a metal core printed circuit board (MC-PCB). The soldering process was carried out by a lead-free Sn/Ag eutectic solder paste; in particular, we focused our attention to non-optimized processes having temperature profiles which gave rise to large density of voids.

A void map has been obtained for each of the four cells by X-ray inspection. One of these maps has been used as input parameter for a thermal finite element analysis (FEA), carried out by means of ADINA 8.7 (Automatic Dynamic Incremental Nonlinear Analysis) software. As a result we have obtained the temperature map of the selected solar cell, exhibiting hot spots in correspondence to the location of voids. This map has then been used as input data for the subsequent electrical analyses performed by ORCAD PSPICE software. To this purpose a distributed 2.5 D electrical model of the solar cell has been implemented; the entire solar cell has been represented by an array of subcells whose PSPICE netlist has been generated through a MATLAB script. In this way solar cell electrical performances have been evaluated.

Further simulations have been performed for regularly spaced void patterns. In particular, we have analysed 2×2 and 10×7 void matrices, for different values of void percentage and sink temperature.

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We have also developed an analytical thermal model useful to assess the local temperature increase of the device surface due to a single isolated void and the whole device thermal resistance in presence of a regular void pattern. The obtained results have been compared to those of finite element analyses.

2. Electrical model

One of the main steps of this work consists of assessing solar cell performances in terms of delivered power under real operating conditions. A detailed description of the equivalent electrical model employed for simulations can be retrieved in Ref.[6,7]. Basically, the solar cell has been divided into a large number of subcells through a nonlinear binning procedure. Each element has then been represented by an equivalent electrical circuit, as shown in Fig. 1.

This model takes into account the main layers that compose a conventional silicon solar cell, i.e., emitter, base, front contact grid and back contact. Each subcell is equipped with a current generator simulating the local photogenerated current, while a diode models the *p–n* junction behaviour. The electrical parameters of the subcells and the geometry of the front contact have been obtained from the devices under test. In order to include in the simulations the device local temperature increases, the electrical parameters of the subcell elements, such as semiconductor layer resistivity and *p–n* junction inverse saturation current, have been calculated depending on the specific temperature value of each grid element, retrieved from the temperature maps.

The temperature coefficient of resistance (TCR), for both the emitter and base, has been calculated as a function of dopant concentrations, according to another work [8]. Table 1 reports the main parameters of the devices under test at room temperature. The cells under test show a comb-like front contact grid pattern composed of 10 μm-wide 5 μm-thick fingers and two 700 μm-thick busbars, for a total coverage of 15%; the current is supposed to be extracted by two 3 mm-wide pads from one side of the cell. In the electrical simulations we have modelled the voids, which are localized in the solder joint region, as discontinuities in the connection between the solar cell back contact and the MC-PCB. To this end the void map obtained by X-ray inspection has been used as an input parameter for the simulations; the obtained solar cell model result composed of 158×215 grid elements. The results of the electrical model simulation comprehend maximum power delivered by the cell, fill factor and open-circuit voltage.

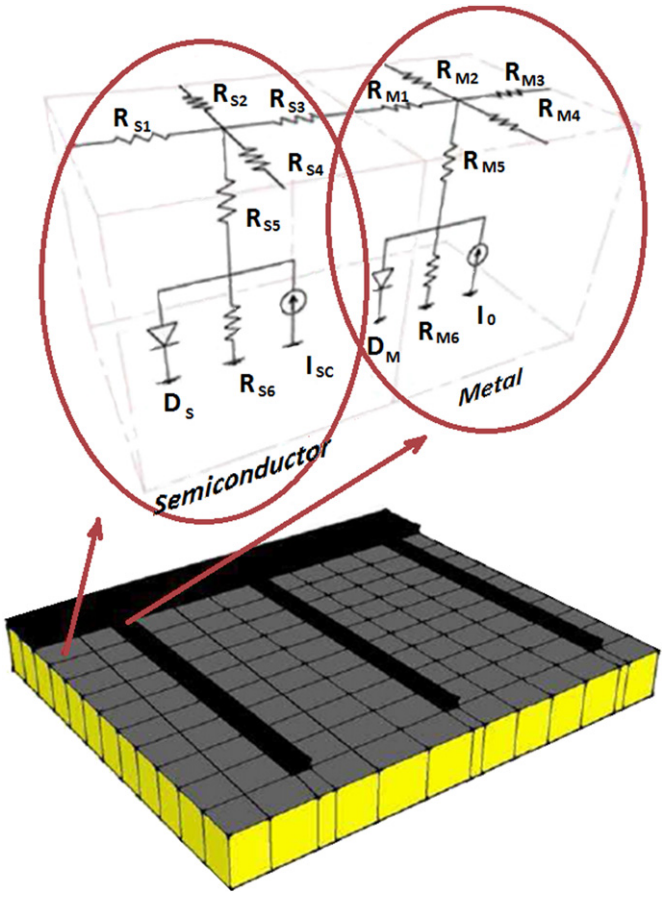

Fig. 1. Pictorial representation of the 2.5D distributed solar cell electrical model.

3. Thermal model

3.1. Analytical approach

In this paragraph we will obtain an analytical expression for both the steady-state local temperature increase at cell surface and the device thermal resistance increase caused by a single void in the die attach layer, by using the simplified model described below. Furthermore, the whole device thermal resistance, in presence of a matrix of *N* identical voids, has been estimated using the same model.

For an easy geometrical treatment we have considered the thermal resistance and temperature increase due to a cylindrical shaped void lying in the device solder region, having a radius of base *R* and the same thickness of the solder joint. Moreover we have assumed that the heat flux *F*, due to solar irradiance, is entirely injected at the top surface of the device. The thermal conduction through void volume has been neglected since the air thermal conductivity – $k_{air}=0.0257\ \mathrm{W\ m^{-1}\ K^{-1}}$ at 300 K – is about four orders of magnitude smaller than that of silicon – $k_{Si}=148\ \mathrm{W\ m^{-1}\ K^{-1}}$ at 300 K – in the temperature range of interest. As a consequence the heat flux *F* does not flows across the void volume but instead it spreads out toward the boundary regions and is eventually dissipated in the direction beneath the copper layer.

As a working hypothesis we consider that the temperature vertical gradient is zero inside the silicon cylinder above the void volume. This introduces a small error in our model but allows us to obtain an approximate analytical form of the temperature rise caused by solder joint discontinuities. Due to void presence, the heat flux generated at the top surface of the silicon cylinder spreads across the plane of the device, i.e., the *xy* plane in Fig. 2, from the inner side of the silicon cylinder to its edge.

A further approximation consists of considering the heat flux exiting the cylindrical silicon volume above the void to be directly sunk toward the beneath copper layer, without spreading into the surrounding regions. This approximation does not reflect any realistic case since a temperature increase is always experienced by the device

Table 1
Room temperature parameters used for the electrical simulations.

Cell dimensions	$1.9\ \mathrm{cm} \times 1.4\ \mathrm{cm}$
Short-circuit current density	$3\ \mathrm{A/cm^2}$
Emitter resistivity	30 Ω/sq
Bulk resistivity	1 Ω cm
Concentration factor	100 ×
Metal-semiconductor resistivity	$1 \times 10^{-6}\ \Omega\ \mathrm{cm^2}$
Metal resistivity	$2.82 \times 10^{-6}\ \Omega\ \mathrm{cm}$
Emitter thickness	300 nm
Bulk thickness	250 μm