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Effective Schottky barrier height lowering technique for InGaAs contact scheme: D_{MIGS} and D_{it} reduction and interfacial dipole formation

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ABSTRACT

The excellent Schottky barrier height (SBH) lowering effect of the metal/$In_{0.53}Ga_{0.47}As$ contact is demonstrated to achieve extremely low contact resistance for n-channel $In_xGa_{1-x}As$-based devices. Severe Fermi-level pinning, caused by large amounts of metal-induced gap states (MIGS) and interface states at the $In_{0.53}Ga_{0.47}As$ surface, can be effectively alleviated, and the large SBH of the metal/$In_{0.53}Ga_{0.47}As$ interface can be significantly lowered by introducing a metal-interlayer-semiconductor (MIS) structure, with the insertion of an Al-doped ZnO (AZO)/Ge interlayer stack between the metal and the $In_{0.53}Ga_{0.47}As$. The AZO interlayer is used as a heavily doped interlayer to reduce the MIGS, decrease its tunneling thickness, and lower the SBH. Reduction of the interface states at the $In_{0.53}Ga_{0.47}As$ surface is achieved by adopting an ultrathin Ge layer as the surface passivation layer. Furthermore, a favorable interfacial dipole is formed at the AZO/Ge/$In_{0.53}Ga_{0.47}As$ interfaces, which induces further SBH lowering and reduction of the AZO tunneling thickness. A below zero effective SBH for a Ti/AZO (1.2 nm)/Ge (0.5 nm)/n^+-$In_{0.53}Ga_{0.47}As$ ($N_d = 1 \times 10^{19}\,cm^{-3}$) structure is estimated while the SBH of the Ti/n^+-$In_{0.53}Ga_{0.47}As$ structure is 0.27 eV. A specific contact resistivity value of $(8.3 \pm 2.6) \times 10^{-9}\,\Omega\,cm^2$ is achieved for the proposed MIS structure, which is one of the lowest reported values for ohmic contacts to date. This result suggests that the proposed MIS structure, incorporating the AZO/Ge interlayer stack, presents a promising ohmic contact technique for III–V compound semiconductor-based applications.

1. Introduction

Silicon (Si) based complementary metal-oxidesemiconductor (CMOS) technology has limited applications due to its physical problems. To overcome these challenges, the use of alternative channel materials to Si, such as III–V compound semiconductors and germanium (Ge), has gained increasing importance [1]. In particular, III–V compound semiconductors are promising candidates for use in n-channel high-switching-speed devices, such as metal-oxidesemiconductor field-effect transistors (MOSFETs), high-electron-mobility transistors (HEMTs), and quantum-well field-effect transistors (QW FETs), owing to their excellent carrier transport properties [2–5]. Among the III–V semiconductors, InGaAs has high electron mobility and can be grown on Si, InP, and GaAs substrates with little lattice mismatch, by modulating the In and Ga mole fraction, thereby reducing the manufacturing cost, which makes it a sound material for high-performance next-generation transistor technologies [5].

However, current III–V semiconductor-based devices have not exhibited better performance than Si-based devices, because their source/drain (S/D) contact technique, which is a serious problem, has not yet been optimized. Considering nanometer-scale features, optimizing the S/D contact resistance becomes one of the most significant requirements in the manufacture of high-performance devices. Therefore, the need for further study of S/D contact techniques is apparent. Most ohmic contact formation techniques for III–V semiconductor-based devices currently include thermal annealing processes to form alloyed contacts, such as Au–Ge based contacts for MOSFETs [6–8], and Pd/Ge/Ti/Au contacts for HEMTs [9]. However, these thermal processes can cause an inadvertently large S/D contact region, poor surface morphology, and variable electrical S/D contact properties [10]. Thus, the drawbacks of these alloyed contact processes limit the scalability of III–V semiconductor transistors, add further obstacles to the ensuing fabrication process, and degrade the device performance [10]. Therefore, several non-alloyed ohmic contact schemes such as Ti/Pd/Au [11], Mo [12], and W [13] contacts on III–V semiconductors have been developed recently, to improve the electrical performance of InGaAs-based transistors. Nevertheless, the reduction of contact resistance by simply stacking metal layers directly onto semiconductors is difficult

Abbreviations: SBH, Schottky barrier height; MIGS, metal-induced gap states; MIS, metal-interlayer-semiconductor

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because of severe Fermi-level pinning at the metal/III-V semiconductor contact interface [4,14]. When the metal is in direct contact with the $In_{0.53}Ga_{0.47}As$ surface, the Fermi-level on the metal side of the interface tends to be pinned to the charge neutrality level (CNL) of the $In_{0.53}Ga_{0.47}As$, regardless of the metal's own workfunction [15]. Especially, the narrower the bandgap of the semiconductor becomes, the more severe the Fermi-level pinning problem becomes [15]. Thus, the metal/$In_{0.53}Ga_{0.47}As$ contact exhibits a large Schottky barrier height (SBH) because the CNL of the $In_{0.53}Ga_{0.47}As$ is located near the mid-gap (i.e., 0.27 eV below the conduction band minimum for $In_{0.53}Ga_{0.47}As$, a material widely investigated for n-channel devices) [16]. To achieve an ultralow contact resistance, the electron SBH should be reduced to form an ohmic contact for $In_{0.53}Ga_{0.47}As$ through effective Fermi-level unpinning. To accomplish this, the two main causes of the Fermi-level pinning in $In_{0.53}Ga_{0.47}As$—i.e., metal-induced gap states (MIGS) and interface states at the semiconductor surface—should be eliminated [17].

1.1. Reduction of D_{MIGS}

MIGS are generated when the electron wave function from the metal side penetrates the semiconductor at the metal/semiconductor interface [17]. This can be blocked by the insertion of wide bandgap dielectric layers, such as SiN, Al_2O_3, ZrO_2, TiO_2, and ZnO, between the metal and the semiconductor [18–20]. It has been demonstrated recently that the metal-interlayer-semiconductor (MIS) structure mainly on Si or Ge substrates considerably reduces the contact resistance by inducing Fermi-level unpinning and a lowering of the SBH, as shown in Fig. 1. However, when the interlayers, which have low electron affinity such as SiN, SiO_2, and Al_2O_3, are inserted between the metal and the semiconductor, there are limits to reduce the contact resistance due to their large tunneling barrier for electrons [15]. As shown in Fig. 1b, to lower the tunneling barrier and improve the conduction through the interlayer between the metal and the semiconductor, proper interlayers, which have a low conduction band offset (CBO) relative to semiconductors (i.e., Si, Ge, and III–V semiconductors), are necessary. For this reason, TiO_2 and ZnO have been adopted as the interlayer owing to their low CBO properties to semiconductors [21–23].

1.2. Reduction of D_{it}

In addition to MIGS, the effect of the interface state density, D_{it}, on the Fermi-level pinning is also significant. Thus, to lower the effective SBH, reduction of D_{it} at the semiconductor surface is also necessary [14]. In the III–V semiconductors, because native oxides typically yield a poor interface quality corresponding to high D_{it}, a reliable surface passivation technique is required. Several approaches of passivating the interface have been reported in literature, such as chemical pretreatment methods using $(NH_4)_2S$, HCl, or NH_4OH solutions; CF_4 or SF_6 plasma; and the intentional deposition of interface passivation layers (IPLs) such as Si and Ge [14,24–27]. However, these chemical pretreatment methods are inadequate because they are not permanent surface passivation methods. Meanwhile, the insertion of IPLs can effectively reduce D_{it} with permanent suppression of the native oxide formation, even if the oxide layer, as the interlayer, is formed on top of the IPL. For this reason, the IPLs such as ultrathin Si and Ge layers, have been suggested for the purpose of suppressing the formation of Ga–O and As–O bonding responsible for increasing D_{it} [26,27].

1.3. Interfacial dipole formation

An interfacial dipole formation between two different dielectric layers can tune the band alignment by producing a local electric field [28,29]. When two different dielectric materials are directly in contact, the oxygen ions at the layer with higher oxygen areal density (σ) diffuse into the layer with relatively low σ, which induces the interfacial dipole. For the MIS structure with the IPL, the interfacial dipoles at the interlayer/IPL and IPL/$In_{0.53}Ga_{0.47}As$ interfaces are formed because there are local oxygen ion diffusions caused by σ differences of each stack [30,31]. Therefore, a selection of suitable material for IPL that can induce a dipole in a favorable direction leading to reduced SBH and suppress the native oxide formation should be carefully considered. The proper interlayer/IPL stack can remarkably lower the SBH by reducing both D_{MIGS} and D_{it}, and forming the favorable interfacial dipole.

In this paper, we develop an effective SBH lowering technique, based on the MIS structure for n-type $In_{0.53}Ga_{0.47}As$, to lower the SBH and achieve ultralow contact resistance. We focus on the reduction of D_{MIGS} and D_{it} and the interfacial dipole formation by insertion of an AZO/Ge interlayer stack between the metal and the $In_{0.53}Ga_{0.47}As$. Based on our electrical and X-ray photoelectron spectroscopy (XPS) analyses, the significant SBH lowering effects and the contact resistance reduction for n-type $In_{0.53}Ga_{0.47}As$ are well demonstrated.

2. Experimental details

The Si-doped n^+-type $In_{0.53}Ga_{0.47}As$ ($N_d = 1 \times 10^{19}\,cm^{-3}$) epitaxial layer was grown by metal-organic chemical vapor deposition (MOCVD) on InP wafers, to match the lattice constant. The surfaces of the $In_{0.53}Ga_{0.47}As$ substrates were cleaned sequentially by acetone, 2-propanol, and deionized water, and subsequently wet cleaned to remove native oxides using a 29% NH_4OH solution for 3 min. The clean substrates were immediately passivated with an aqueous $(NH_4)_2S$ solution for 1 min. Ultrathin Ge IPLs were then deposited by an e-beam evaporator, and thin ZnO and Al-doped ZnO (AZO) layers were deposited by atomic layer deposition (ALD). The ZnO layer was formed using a diethyl zinc (DEZ) precursor and a H_2O gas reactant in 150 °C chamber temperature conditions. The AZO layer was optimized by modulating the process temperature and ZnO/Al_2O_3 cycles. The ALD cycles of the DEZ/trimethylaluminum (TMA) precursors were determined with a 6:1 ratio at a process temperature of 150 °C, to form an

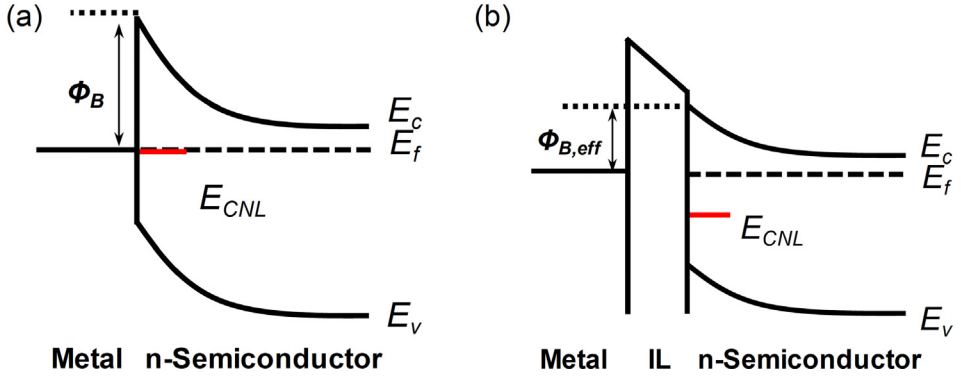

Fig. 1. Energy band diagrams of (a) the metal/n-semiconductor MS contact and (b) the metal/interlayer (low CBO)/n-semiconductor MIS contact.

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