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Density-functional theory molecular dynamics simulations of a-HfO_2/a-SiO_2/SiGe and a-HfO_2/a-SiO_2/Ge with a-SiO_2 and a-SiO suboxide interfacial layers

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ABSTRACT

Comprehensive Density-Functional Theory (DFT) Molecular Dynamics (MD) simulations were performed to investigate interfaces between a-HfO_2 and SiGe or Ge semiconductors with fully-stoichiometric a-SiO_2 or sub-oxide SiO interlayers. The electronic structure of the selected stacks was calculated with a HSE06 hybrid functional. Simulations were performed before and after hydrogen passivation of residual interlayer defects. For the SiGe substrate with Ge termination prior to H passivation, the stacks with a-SiO suboxide interlayer (a-HfO_2/a-SiO/SiGe) demonstrate superior electronic properties and wider band-gaps than the stacks with fully coordinated a-SiO_2 interlayers (a-HfO_2/a-SiO_2/SiGe). After H passivation, most of the a-HfO_2/a-SiO_2/SiGe defects are passivated. To investigate effect of random placement of Si and Ge atoms additional simulations with a randomized SiGe slab were performed demonstrating improvement of electronic structure. For Ge substrates, before H passivation, the stacks with a SiO suboxide interlayer (a-HfO_2/a-SiO/Ge) also demonstrate wider band-gaps than the stacks with fully coordinated a-SiO_2 interlayers (a-HfO_2/a-SiO_2/Ge). However, even for a-HfO_2/a-SiO/Ge, the Fermi level is shifted close to the conduction band edge (CBM) consistent with Fermi level pinning. Again, after H passivation, most of the a-HfO_2/a-SiO_2/Ge defects are passivated. The stacks with fully coordinated a-SiO_2 interlayers have much stronger deformation and irregularity in the semiconductor (SiGe or Ge) upper layers leading to multiple under-coordinated atoms which create band-edge states and decrease the band-gap prior to H passivation.

1. Introduction

Although Ge is less popular in semiconductor transistor applications than Si, Ge has compelling properties for scaled low power electronics. Ge is one of a few semiconductors that can provide significantly higher hole mobility than Si and, therefore, is being extensively investigated for p-channel metal-oxide-semiconductor-field-effect-transistors (MOSFET). SiGe alloys provide a compromise in terms of higher hole mobility and ease of integration onto Si wafers and facile strain engineering [1]. Enhanced transport features with p-type metal-oxide-semiconductor (PMOS) in SiGe fin field-effect transistor (FinFET) structures include very high hole mobility (457 $cm^2 V^{-1} s^{-1}$) for SiGe with 65–70% Ge composition [2,3].

The structural properties of amorphous oxide/semiconductor interfaces are important since they impact the electrical properties and reliability of MOSFET devices. Currently amorphous a-HfO_2 is the most widely employed high-K MOSFET gate oxide for Si channels; it is used as a substitute for traditional a-SiO_2 gate oxide to reduce gate leakage for a fixed equivalent oxide thickness. However, direct interfaces between Si and HfO_2 degrade mobility and induce threshold shifts in MOSFETs [4]. Conversely, the Si-SiO_2-HfO_2 interface uses a subnanometer SiO_2 interlayer to reduce remote phonon scattering and Si dangling bonds, thereby creating better mobility and threshold voltage [4–8]. In the present work, the effect of a-SiOx interlayer insertion between HfO_2/SiGe was investigated to obtain low interface defect density. The present DFT-MD simulations provide detailed atomistic insight into the physical processes in the a-HfO_2/a-SiOx/SiGe and a-HfO_2/a-SiOx/Ge interfaces logically complementing experimental research and providing directions for further improvement of interface processing.

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2. Stack formation and simulation procedure

All DFT simulations were performed with the Vienna *ab initio* simulation package (VASP) using projector augmented-wave (PAW) pseudopotentials (PPs) and the Perdew–Burke–Ernzerhof (PBE) exchange-correlation functional [9–14]. The *a*-HfO_2 sample was stoichiometric and included 40 Hf and 80 O atoms. Several a-HfO_2 samples were generated using hybrid classical and DFT-MD simulations including annealing, cooling and relaxation. The amorphous sample quality was verified via radial-distribution function (RDF) main peak positions, average nearest neighbor numbers, nearest neighbor distributions, and DFT calculated band-gaps demonstrating good correlation to available simulated and experimental reference properties [15–20]. The sample with the best match to experimental data was selected and used for simulations. The amorphous samples were generated to match the Ge(001) surface area and used for both Ge(001) and SiGe (001) since their lattice constants differ only by 3%. A more detailed explanation of a-HfO_2 sample generation was presented elsewhere [21].

The $Si_{0.5}Ge_{0.5}$ unit cell with an ordered checkerboard placement of Si and Ge atoms and the Ge unit cell were relaxed at variable volume to obtain DFT lattice constants. The initial a-SiO/SiGe slab was built including 5 Si and 5 Ge layers (8 atoms per layer) terminated by a layer of Ge atoms. To form the a-SiOx layer, 2 additional Si layers (16 Si atoms) were placed on top of the Ge-terminated SiGe and 16 O atoms were randomly placed inside and above of these 2 upper Si layers. Ge termination of SiGe was chosen since this is the most challenging case for passivation, and Ge is known to segregate to the surface of SiGe in UHV. The three bottom layers of SiGe were permanently fixed in bulk-like positions, and the bottom surface was passivated by H atoms to simulate continuous bulk. The stack was DFT-MD annealed at 800 K for 1000 fs (with 1 fs timestep), cooled to 0 K for 200 fs and relaxed to the ground configuration below 0.05 eV/Å force-tolerance level. To form the a-SiO_2/SiGe slab, 16 more O atoms were placed on the previous slab and annealed, cooled, relaxed according to the same procedure. To investigate effect of Si and Ge random placement, a randomized SiGe slab was built and prepared in the same way as described above keeping Si/Ge ratio equal to 1:1. The upper surface of randomized SiGe slab has 4 Si and 4 Ge atoms. The a-SiO and a-SiO_2 layers were generated on randomized SiGe slab by DFT molecular dynamics using the same procedure.

The initial a-SiO/Ge slab was built using similar procedure. It included 10 Ge layers (8 atoms per layer) with 2 additional top Si layers (16 Si atoms) and 16 O atoms randomly placed on top and inside 2 upper Si layers. The three Ge bottom layers were permanently fixed in bulk-like positions, and the bottom surface was passivated by H atoms. The a-SiO/Ge stack was DFT-MD annealed using the same procedure as for the a-SiO/SiGe slab. To form a-SiO_2/Ge slab, 16 more O atoms were placed on the final a-SiO/Ge slab and annealed, cooled, relaxed according to the same procedure.

To simulate oxide-semiconductor stacks, the same a-HfO_2 sample was placed on a-SiO/SiGe (ordered), a-SiO_2/SiGe (ordered), a-SiO/Ge, a-SiO_2/Ge slabs to have interfacial bond lengths close to equilibrium values. The HfO_2 upper surface was terminated by H atoms to passivate significantly under-coordinated Hf atoms. All 4 stacks were DFT simulated using the same procedure. The stack simulation was started with partial initial relaxation with 50 conjugate-gradient (CG) relaxation steps. The goal of the initial relaxation is not a complete relaxation of the stack, but partial alleviation of initial internal stresses produced by oxide stacking.

The stacks were DFT-MD annealed at 800 K for 2000 fs with 1 fs time steps. The total energy of the stacks was plotted over time. Within the final 500 fs of annealing, 3 major energy minima were selected for every stack and corresponding system snapshots were used as starting points for subsequent cooling. This procedure produced 3 systems for every stack. Although these annealing energy minima correspond to the system in excited state at 800 K, and the overall ensemble is non-adiabatic maintaining constant temperature by atom velocity rescaling every 5 timesteps; consequently, the system configurations at these energy minima are reasonable starting points for subsequent cooling and relaxation. For the a-HfO_2/a-SiO/SiGe stack, the 3 selected cooling starting points were: 1912, 1947 and 1970 fs of annealing while for the a-HfO_2/a-SiO_2/SiGe stack the 3 cooling starting points were: 1912, 1945 and 2000 fs of annealing. For the a-HfO_2/a-SiO/Ge stack, the 3 selected cooling starting points were: 1746, 1870 and 2000 fs of annealing while for the a-HfO_2/a-SiO_2/Ge stack, the 3 cooling starting points were: 1574, 1763, and 1885 fs of annealing. The total energy for a-HfO_2/a-SiO_2/Ge during annealing is presented in Fig. 1.

Starting from the 3 selected energy minima for the last 500 fs of annealing, the stacks were cooled to 0 K for 200 fs and relaxed to the ground state below 0.05 eV/Å force-tolerance level. To increase computational performance, the previous simulations were performed at 2 K-points (Gamma and (0.5, 0.5, 0.5)). After final relaxation, the K-point sampling was increased to 3 × 3 × 1, and the stacks were re-relaxed producing very minor changes in geometry but improving electronic structure accuracy.

The total energies of the stacks after final relaxation are summarized in Table 1, and the final geometries of all 12 stacks are presented in Supplementary Materials Figs. S1–S4. It can be seen that final total energies are very close to each other for various annealing times for a given stack, with minor exception for a-HfO_2/a-SiO/Ge case which has difference around 2 eV for different annealing times. The analysis of final stack geometries indicates strong similarity for every stack type consistent with geometry convergence (Supplementary Materials Figs. S1–S4).

After final relaxation, the total energies of all 12 stacks summarized in Table 1 were analyzed to choose the stacks with the minimal energy for every stack type. The selected stacks are presented in Figs. 2 and 3 and include a-HfO_2/a-SiO/SiGe (1970 fs of annealing), a-HfO_2/a-SiO_2/SiGe (2000 fs of annealing), a-HfO_2/a-SiO/Ge (2000 fs of annealing) and a-HfO_2/a-SiO_2/Ge (1574 fs of annealing). To investigate effect of Si/Ge randomization in the SiGe slab, similar simulations were performed with a randomized SiGe slab. The a-HfO_2/a-SiO/SiGe (random) and a-HfO_2/a-SiO_2/SiGe (random) stacks were partially relaxed with 50 GG steps, annealed at 800 K for 2000 fs, cooled to 0 K for 200 fs and relaxed to the ground state configuration below 0.05 eV/Å force-tolerance level. Final

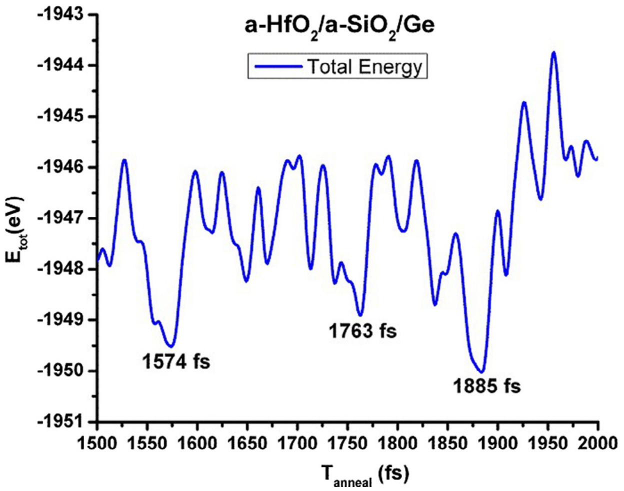

Fig. 1. Total energy for an a-HfO_2/a-SiO_2/Ge stack during last 500 fs of annealing.