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Edge chipping of silicon wafers in diamond grinding

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ABSTRACT

Although diamond grinding is the most commonly used machining technique in silicon wafer thinning, it often induces edge chipping which leads to wafer breakage. This study investigates edge chipping of silicon wafer in diamond grinding. The study correlates edge chipping with the crystallographic orientation and thickness of a silicon wafer, as well as grinding process conditions, such as wheel grit size, grinding mode and feed rate. It identifies edge chipping in terms of critical thickness, geometry and dimensions. The study discusses the mechanisms of edge chipping based on machining mechanics and energy theories. Conclusions are drawn to summarize the study.

0. Introduction

The demand for miniaturized and highly integrated systems is dramatically increased in portable electronic products, such as mobile phones, integrated circuit (IC) cards, and digital cameras. Using integrated circuit chips with multi-layer structures and low-profile package is a cost effective solution to making these products in which a silicon wafer is thinned down to several tens of micrometers from 725 μm for 8 inch wafers or 775 μm for 12 inch wafers to meet the package requirements. In a wafer thinning process, diamond grinding is usually adopted simply because of its ability to provide high throughput, quality, and dimensional accuracies. Studies on diamond grinding machines, diamond wheels and grindability have been extensively reported and reviewed [1–5]. Previous studies have demonstrated that surface and subsurface damage is inevitably produced in grinding of silicon wafers [6–8]. Damage in the form of residual stresses results in severe wafer warpage and further breakage, which puts a limit to the minimum thickness of a silicon wafer during the thinning process [9–12]. Residual stresses are generally considered an important cause of wafer breakage and a limiting factor to the minimum wafer thickness. In addition, there is another equally important cause of wafer breakage, i.e., edge chipping. Practically, the prime wafer edge is machined to a rounded shape for strength considerations. However, the round edge is turned into a sharp edge in the wafer thinning process, as shown in Fig. 1, which undermines the edge strength. Chipping easily occurs along the sharp edge, leading to edge fluttering and even wafer breakage. Edge chipping has thus become a significant issue in wafer grinding and deserves investigations. Unfortunately, the edge chipping issue has long been ignored. The mechanisms for edge chipping are not well understood, which puts out effort in manufacturing ultra-thin wafers by grinding under jeopardy.

This study aims to experimentally investigate the edge chipping issue of silicon wafers in the thinning process with a diamond grinding wheel. The study discusses how edge chipping is related to grinding conditions, wafer thickness, and crystal orientation of a wafer subjected to grinding.

1. Experimental details

1.1. Wafer grinding experiment

All grinding experiments were performed on a wafer grinder (VG401 MK II, Okamoto, Japan). Cup-type grinding was adopted in accordance with the principle of wafer rotation grinding. An on-line thickness measurement device was incorporated into the grinding system to monitor wafer thickness. Resin-bond diamond wheels (Asahi, Japan) with respective grain sizes of 600, 2000 and 3000 were used in the experiments. Polished monocrystalline (1 0 0) silicon wafers (150 mm diameter) with thickness of about 700 μm were ground with deionized water as grinding coolant. Grinding conditions are given in Table 1.

Fig. 2 presents two different grinding modes: down-grinding and up-grinding. When an abrasive grain on the grinding wheel removes the wafer material from the edge to the center along

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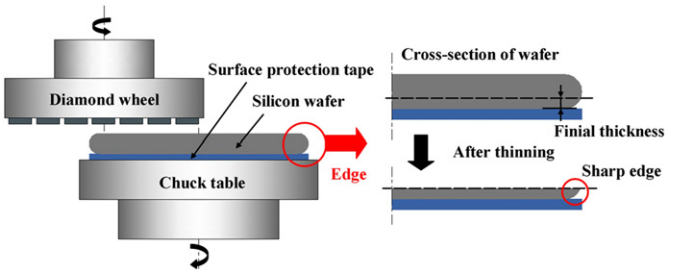

Fig. 1. Illustration of sharp edge formation during silicon wafer thinning process by grinding.

Table 1
Grinding conditions used in the experiments.

Grinding mode	Mesh number	Wheel speed [m/s]	Wafer speed [r/min]	Down-feed rate [μm/min]	Spark-out time [s]
Down-grinding	600	43.59	200	20, 40, 60	10
Down-grinding	2000	43.59	200	15, 30	10
Down-grinding	3000	43.59	200	10, 20	10
Up-grinding	600	43.59	200	20	10
Up-grinding	3000	43.59	200	10	10

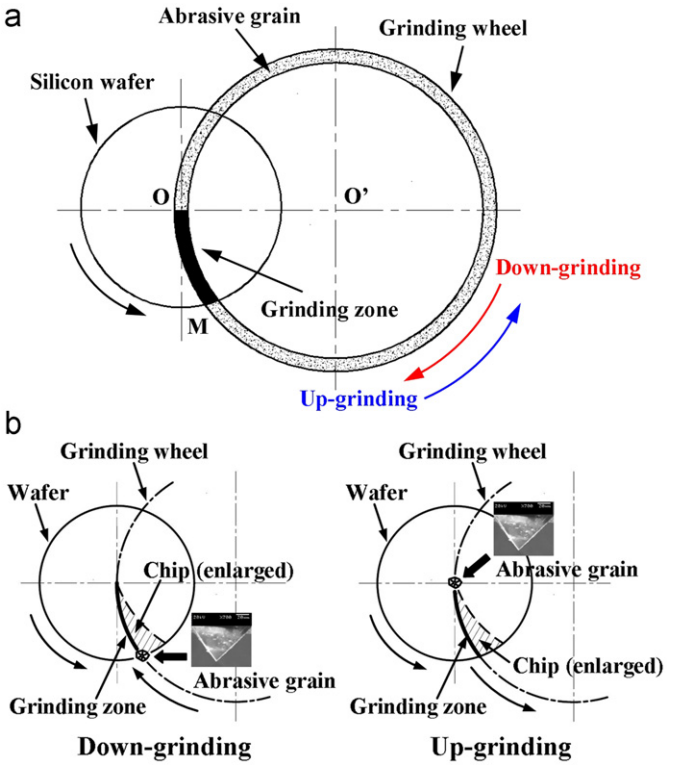

Fig. 2. Illustration of down-grinding and up-grinding, (a) Rotation direction of silicon wafer and grinding wheel in down-grinding and up-grinding, (b) chipping thickness variation in down-grinding and up-grinding.

path MO, the chip thickness decreases from the start of the cut until it is zero at the end of the cut and the mode is called down-grinding; otherwise, it is called up-grinding. In the experiments, all the silicon wafers were thinned by the diamond grinding wheels from the original thickness of 700 μm to 100 μm. Edge chipping was inspected if wafer thickness was further reduced to 50 μm.

1.2. Measurement of edge chipping

Fig. 3 shows a typical edge chipping pattern of a ground silicon wafer. In this study, edge chipping is evaluated using the average chipping width W which was calculated as:

$$W = S/L \tag{1}$$

where L is the sampling length of line AB which runs over the peak point of the edge profile; S is the chipping area surrounded by the edge profile line and line AB, as shown in Fig. 3. Sampling length L and chipping area S was measured by the AutoCAD software. After each grinding experiment, an optical microscope (MX40, Olympus, Japan) was utilized to observe edge chipping. The optical image of edge chipping was then imported into the AutoCAD software for chipping edge-profile approximation and chipping area calculations.

The sampling locations for edge chipping information are shown in Fig. 4. There are eight sampling positions around the wafer edge. The first location is marked location 1, as shown in

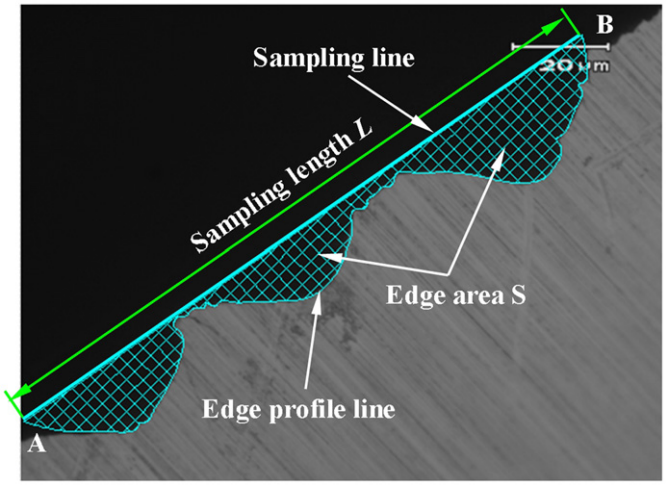

Fig. 3. Edge chipping of silicon wafer induced by grinding.

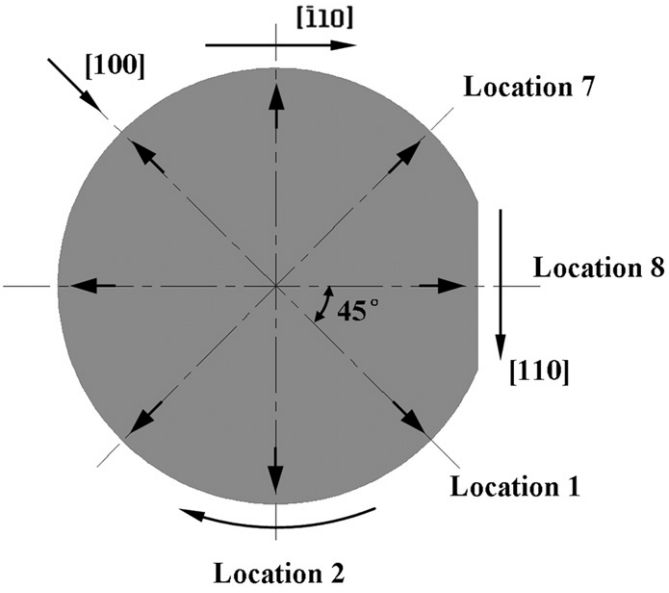

Fig. 4. Sampling locations along wafer edge.