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Fully-transparent graphene charge-trap memory device with large memory window and long-term retention

Sejoon Lee [a, b, *], Youngmin Lee [b], Sung Min Kim [c], Emil B. Song [c]

[a] Department of Semiconductor Science, Dongguk University - Seoul, Seoul 04623, South Korea
[b] Quantum-Functional Semiconductor Research Center, Dongguk University-Seoul, Seoul 04623, South Korea
[c] Department of Electrical Engineering, University of California at Los Angeles, Los Angeles, CA 90095, USA

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ABSTRACT

A fully-transparent graphene-based charge-trap memory device was realized by fabricating a graphene-channel field-effect transistor with high-*k*/low-*k*/high-*k* oxide stacks of $Al_2O_3/AlO_x/Al_2O_3$ and indium-tin-oxide gate/source/drain electrodes on the polyethylene naphthalate substrate (*i.e.*, ITO-gated AXA-gFET). The usage of low-*k* AlO_x as a charge-trap layer allowed us to demonstrate a high-performance memory device, exhibiting a large memory window of ~9.2 V and a tenacious retention of the memory window margin up to ~57% after 10 years. Memory cells comprising the ITO-gated AXA-gFET arrays displayed a high transparency with the average optical transmittance of ~83% in visible wavelength regions. These properties may move us a step closer to the practical application of graphene-based memories for future transparent electronics. In-depth analyses on the electrical characteristics and the mechanisms of the memory functions are presented.

1. Introduction

Graphene has emerged as one of the most promising candidates for future transparent and flexible electronics because of its astonishing physical properties (*e.g.*, a high electron mobility, a high optical transparency, and a high mechanical strength in a two-dimensional lattice structure of sp^2 carbon arrays) [1,2]. Furthermore, a rapid scientific and technical renovation for imminent transparent-, flexible-, and/or wearable-electronics has led to a prosperous interest in graphene and its device applications [3–8]. For the next-generation transparent and flexible electronics, numerous electronic devices (*e.g.*, analog amplifiers, digital logic circuits, memory cells *etc.*) should be realized and even be integrated on a single transparent and flexible substrate. Among various types of transparent and flexible devices, graphene-based non-volatile memories have attracted vast attention because they hold promise for great potential as a mainstream of future memory modules [9]. One tangible scheme for high-performance graphene memory cells is the graphene charge-trap flash memory (CTFM) device because graphene can render several exceptional advantages over conventional silicon-based memory devices (*e.g.*, a high gate-controllability [10,11], a low cell-to-cell interference [12], a large memory window [13–17] *etc.*). Due to the high controllability for both the size and the site of the charge-trap layer, the CTFM device could also enable a placement-dependent multi-level memory functionality [18,19]. In addition, a spectrum of graphene-based memory applications can be further swiftly streamed toward transparent-, flexible-, and/or wearable-electronics through integrating graphene with polymers [20,21] and/or other van der Waals materials [22,23].

In this article, we report on the robust memory characteristics (*i.e.*, an enlarged memory window, a suppressed electron back-injection, an improved data retention *etc.*) of the high-performance fully-transparent graphene-CTFM device. The transparent CTFM devices are devised on the polyethylene naphthalate (PEN) substrate in the form of a graphene field-effect-transistor (gFET) with an oxide stack of $Al_2O_3/AlO_x/Al_2O_3$ (AXA) and a single-layer graphene (SLG) channel. The electrical characteristics of the AXA-gFET CTFM devices are thoroughly examined, and the mechanisms of the memory functions in the fabricated graphene-CTFMs are discussed.

* Corresponding author. Department of Semiconductor Science, Dongguk University - Seoul, Seoul 04623, South Korea.
E-mail address: sejoon@dongguk.edu (S. Lee).

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2. Experimental details

2.1. Preparation of SLG/PEN substrates

SLG was grown on Cu foil using a chemical vapor deposition method [24,25] and transferred onto the surface of the PEN substrate by using a poly (methyl methacrylate) transfer method [26] (see also Fig. 1(a)). The quality of SLG was examined through the Raman scattering spectroscopy measurement by using a Renishaw Micro Raman microscope system. A 514-nm laser was used with an acquisition time of 600 s, and the power density for laser irradiation was less than 2 mW/μm^2. The SLG nanosheet exhibits a typical Raman feature of high-quality SLG [27]; *i.e.*, single Lorentzian peaks at the G and 2D bands with a high intensity ratio of 2D/G (>2) (lower inset of Fig. 1(a)). In addition, the absence of Raman scattering from defect-related D band ($\approx$1350 cm^{-1}) depicts our SLG to be uniformly constructed with the sp^2-hybridized carbon structure [28].

2.2. Fabrication of AXA-gFET CTFM devices

Fig. 1 schematically illustrates the fabrication procedures of the fully-transparent AXA-gFET CTFM device. As a primary task, the SLG channels were patterned *via* photolithography techniques using a SLG sheet transferred on the PEN substrate (Fig. 1(a) and (b)). Next, the source/drain areas were defined through forming indium-tin-oxide (ITO) electrodes by *e*-beam evaporation and lift-off methods (Fig. 1(c)). Thereafter, the gate-oxide stack of AXA was created onto the SLG channel by following processes. First, the Al_2O_3 tunnel oxide layer (~15 nm) was deposited onto the SLG channel by atomic-layer-deposition (ALD) with a naturally oxidized Al_2O_3 seed layer (~1 nm) [29]. Here, we note that all of the ALD processes were performed at low temperature of 110 °C so as not to exceed the glass transition temperature of the PEN substrate (~200 °C). To create the charge-trap layer (*i.e.*, AlO_x) onto the top of the Al_2O_3 tunnel oxide layer, we subsequently carried out an oxygen ion bombardment (OIB) treatment for 30 s at plasma power of 100 W (Fig. 1(d)). Finally, the 25-nm-thick Al_2O_3 control-oxide layer was deposited onto the OIB-treated AlO_x charge-trap layer by using ALD, and the transparent gate electrode was formed by ITO evaporation and lift-off (Fig. 1(e)).

2.3. Characterization of SLG and AXA-gFET CTFM devices

The optical transmittance properties of PEN, SLG/PEN, and AXA-gFET CTFM were measured by using a UV–visible spectrometer (Ocean Optics 2000). The electrical properties and the memory characteristics of the AXA-gFET CTFM devices were measured at room temperature in air atmosphere by using a Keysight B1500A and a Keithley 4200 semiconductor device parameter analyzer systems.

3. Results and discussion

Since the OIB process leads to the generation of charge-traps (*e.g.*, Al and/or O vacancies, interstitials, antisites *etc.*) in aluminum-oxide [30], the AlO_x layer in AXA will act as a charge-storage layer (see Fig. S1). Hence, one can anticipate the present type of the AXA-gFET to operate as a graphene-CTFM device. Namely, the program/erase (P/E) operation will take place on the basis of the electron/hole storage in the AlO_x charge-trap layer. As illustrated in the lower inset of Fig. 1(e), in the program mode, the positive gate-voltage (*i.e.*, $+V_G = V_P » 0$) induces plenty of electrons in the SLG channel, and permits electron-tunneling from SLG into AlO_x. Because the electrons stored in AlO_x decrease an electrochemical potential in AXA (see also Fig. S2), the charge-neutrality point (*i.e.*, Dirac point; V_{Dirac}) will eventually shift toward the positive V_G region [14]. Due to the ambipolar conduction property in graphene, additionally, a similar behavior will also occur for hole carriers under the erase mode (*i.e.*, under $-V_G = V_E « 0$) [14–17]. These allow a memory operation of the AXA-gFET in a wide voltage range, enabling a large memory window of the device (*i.e.*, $\Delta V_M = |+\Delta V_{Dirac|Vp|} + |-\Delta V_{Dirac|Ve|}|$), as discussed later.

Fig. 2(a) and (b) show the scanning electron microscopy images of the CTFM arrays fabricated on the PEN substrate and the SiO_2/Si substrate (*i.e.*, reference sample), respectively, through an identical procedure described above. The arrays of AXA-gFET structures are effectively constructed on the PEN substrate. The AXA stacks

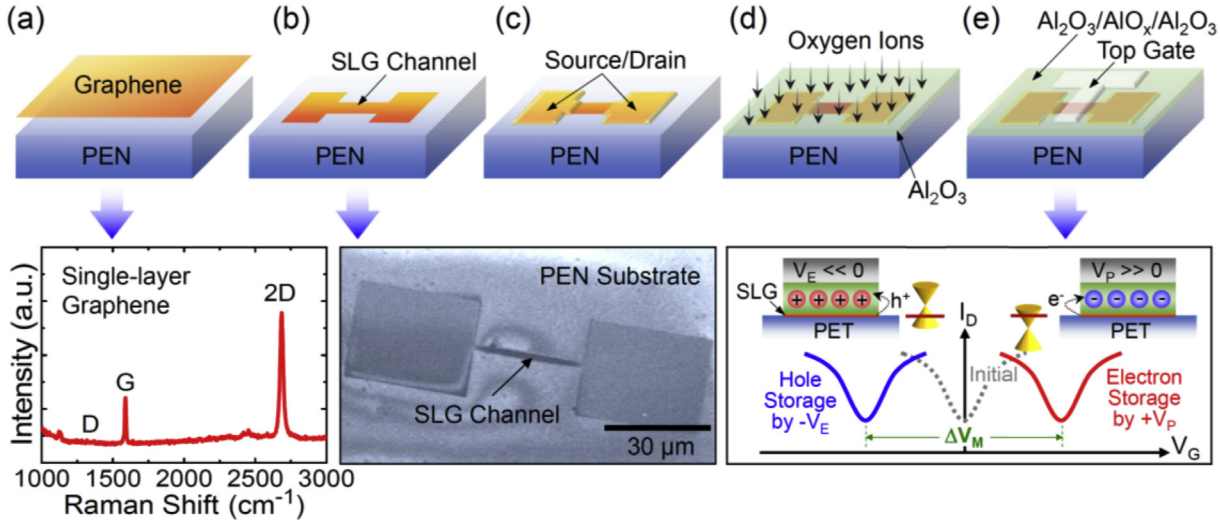

Fig. 1. Fabrication procedures of the fully-transparent AXA-gFET CTFM device on the PEN substrate: (a) Transfer of SLG onto the PEN substrate. (Inset) Raman spectrum of SLG. (b) Defining the channel area by using photolithography. (Inset) Scanning electron microscopy image of the channel area. (c) Formation of source/drain electrode by ITO evaporation. (d) Deposition of the tunnel oxide - Al_2O_3 (~15 nm) by using an ALD method and a subsequent OIB treatment to form the AlO_x charge-trap layer. (e) Deposition of the control oxide - Al_2O_3 (~25 nm) by ALD and the formation of the gate electrode through ITO evaporation. (Inset) P/E operation modes of the AXA-gFET CTFM device, represented on the basis of electron/hole injection behaviors depending on the polarity of the gate voltage. (A colour version of this figure can be viewed online.)