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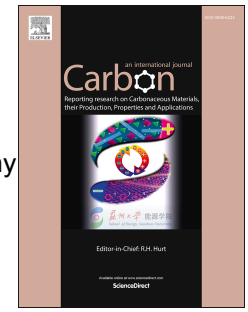

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Fabricating in-plane transistor and memory using atomic force microscope lithography towards graphene system on chip

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Recently, various electronic components including transistor, barristor, memory, and transparent electrode were implemented using graphene. While integrated circuits were demonstrated by combining graphene transistors and passive components, system on chip (SoC) platform, state-of-the-art semiconductor technology, by combining transistors and memories on the same chip, has not yet been demonstrated. The main obstacle of the realization of SoC is the complexity of fabrication processes originated from the process differences between the transistors and the memories. In this study, using simple and clean atomic force microscope lithography, we fabricated both the switching devices and the memories by forming very thin graphene oxide (GO) barriers in mono-layer graphene at the controlled oxidation voltages. Formed with 7 V and 9 V, the lateral graphene/GO/graphene junction devices exhibit switching of Fowler-Nordheim tunneling current and resistive memory behavior, respectively. The combination of high on/off current ratio (~ 1000) of the switching device and nonvolatility of the memory device fabricated by the same process demonstrates the possibility of graphene SoC platform.

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