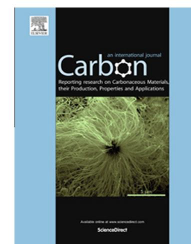
CARBON XXX (2014) XXX–XXX

Available at www.sciencedirect.com
ScienceDirect
journal homepage: www.elsevier.com/locate/carbon



Multilevel resistive memory switching in graphene sandwiched organic polymer heterostructure

Geetika Khurana, Pankaj Misra *, *Ram S. Katiyar* *

Department of Physics, University of Puerto Rico, Rio Piedras San Juan, PR 00936-8377, USA

ARTICLE INFO

Article history:
Received 13 March 2014
Accepted 25 April 2014
Available online xxxx

ABSTRACT

A novel multilevel resistive switching was observed in trilayer stacked geometry composed of graphene nano flakes sandwiched between polyvinylidene fluoride layers fabricated by spin coating method, which are expected to fulfill the need of high density data storage memories. External parameters such as current compliance and induced voltage pulse imposed on the devices provided an aid to tune the inherent resistance states. As fabricated devices exhibited multi level switching with stable resistance ratios between different resistance states having excellent data retention and endurance. Space charge limited conduction and Fowler–Nordheim (F–N) tunneling were found to be responsible for the switching mechanism. Graphene enriched with trapping sites provides the adequate environment for F–N tunneling process to occur, resulting in multi-bit resistance states.

© 2014 Published by Elsevier Ltd.

1. Introduction

Organic memory devices have been intensively researched as the next generation of information storage components due to their simple fabrication, low cost, and flexibility [1,2]. Recently developed organic memories using stacking [3] or flexible concepts with advanced memory architectures [4–7] have enabled practical memory applications. However the major problems with most organic memory devices include slow switching speed [8] and low density storage [9–10] capability which hinders their use for upcoming future needs. It has been reported that performance of existing organic memory devices can be greatly enhanced by forming hybrid organic structures [11], organic/inorganic composites [12] or by dispersing nanomaterials [13,14]. Among all memory devices' concepts, resistive memory devices which are composed of organic/oxide materials sandwiched between two metallic electrodes [15–17] have gained a lot of interest in today's era. The memory effect in resistive switching device is realized through switching of the resistance state of the device between the high and low resistance state and it is controlled by an external electrical stimulus. According to a recent report, two nonvolatile and stable resistance states were observed by applying a suitable bias to polymethyl methacrylate (PMMA) containing sandwiched graphene layer [18], however multilevel switching has not been reported yet. It was also observed that the device without sandwiched graphene layer did not show any switching properties [18]. Among all other organic polymers currently being explored for this application, polyvinylidene fluoride (PVDF) was highly preferred for memory applications primarily due to its non-reactive nature, better heat resistance, flexibility and low weight. Although there have been various reports on ferroelectric switching in PVDF layers, but report on resistive memory switching in PVDF is scanty. As mentioned above, hybrid structures of organic memory devices provide enhanced memory characteristics, therefore, heterostructure of PVDF was fabricated using a charge trapping element in it. Among the various choices for charge trapping layer, use of graphene nano flakes (GR) was considered relevant due to

* *Corresponding authors:* Fax: +1 787 7642571.
E-mail addresses: pankaj.rrcat@gmail.com (P. Misra), rkatiyar@hpcf.upr.edu (R.S. Katiyar).
http://dx.doi.org/10.1016/j.carbon.2014.04.085
0008-6223/© 2014 Published by Elsevier Ltd.

Please cite this article in press as: Khurana G et al. Multilevel resistive memory switching in graphene sandwiched organic polymer heterostructure. Carbon (2014), http://dx.doi.org/10.1016/j.carbon.2014.04.085

their unique chemical structure and excellent properties [19–24] that provides promising opportunities for charge trapping [25] and storage [26] media for memory devices. In addition the defects (vacancy, interstitial sites, residual oxygen, etc.) present in GR can also act as the charge trapping sites [27]. In this paper we report, to the best of our knowledge for the first time, multilevel nonvolatile resistance switching in the graphene sandwiched between PVDF layers. Current compliance parameter and induced voltage pulse technique of suitable amplitude provided an aid to achieve multilevel states during the switching process.

2. Experimental

2.1. *Sample preparation and characterization*

Trilayer structure was fabricated by assembling graphene nano flakes (GR) between PVDF polymer layers through spin coating process. Commercially available ITO coated glass was used as substrate after cleaning it in acetone and then in distilled water using ultrasonicator. Graphene oxide (GO) was synthesized following the same route as in our previous study [28]. In brief, the precursors used were graphite powder, sodium nitrate ($NaNO_3$), concentrated sulphuric acid (H_2SO_4) and potassium dichromate ($K_2Cr_2O_7$). The GO slurry obtained after washing was dispersed in double distilled water and then sonicated for 2 h. Reducing agent hydrazine monohydrate was used to obtain graphene (GR) from GO. PVDF was dissolved in N-methyl-2-pyrrolidone (NMP) while stirring to prepare the PVDF dispersion having concentration ~10 mg/ml. Spin coating was performed to get a sandwich layer of graphene between the polymer layers. Briefly, 50 μl of PVDF solution was dropped onto the ITO substrate and was given a wetting time of 10 s and then performed spinning at 600 rpm for 30 s followed by 1200 rpm for 30 s to deposit a layer of PVDF. This process was repeated until the desired thickness was obtained. In similar manner the layer of GR was deposited on the bottom layer of PVDF and finally again PVDF was deposited on GR to get sandwich structure geometry. The total estimated thickness of the structure obtained was ~80 nm. The film was then baked at 140 °C for 1 h. Finally, DC sputtering was used to deposit Platinum top electrode having area $100 \times 100\ \mu m^2$ through shadow mask to obtain devices from the stacked structure. Current–Voltage (*I–V*) measurements were performed using Keithley 2401 in top–bottom configuration.

3. Results and discussion

The simple metal–insulator-metal (MIM) structure containing graphene nano flakes (GR) embedded in PVDF layer compiles the insulator part for MIM (see Section 2), which was sandwiched between ITO bottom electrode and Platinum (Pt) top electrode as shown in Fig. 1. This geometry was used to investigate non-volatile resistive memory switching.

Typical *I–V* characteristics of the fabricated device were performed at room temperature as shown in Fig. 2. Voltage was swept from $0\,V \rightarrow +V_{max} \rightarrow 0\,V \rightarrow -V_{max} \rightarrow 0\,V$ in the steps of 0.1 V. Initially the device was in high resistance state

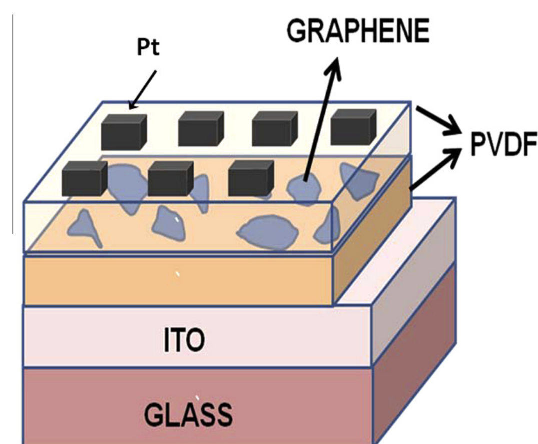


Fig. 1 – Schematic diagram of the layer by layer fabricated Pt/PVDF/GR/PVDF/ITO memory devices. Top electrode of Platinum (Pt) having area $100 \times 100\ \mu m^2$ was deposited using DC sputtering. (A color version of this figure can be viewed online.)

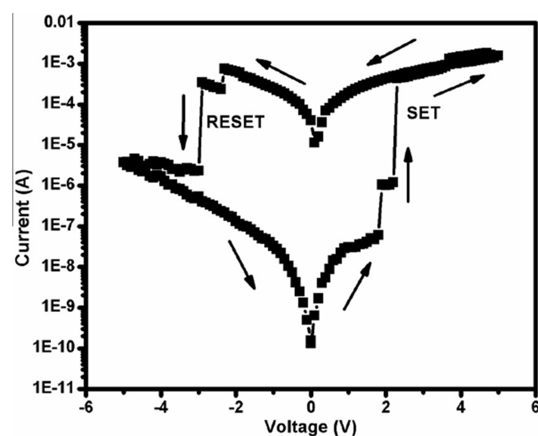


Fig. 2 – Typical *I–V* characteristics of the Pt/PVDF/GR/PVDF/ITO memory device in voltage sweep mode at ambient condition. *I–V* curves are plotted in semilogrithmic scale.

(HRS). As the positive voltage on the top electrode was increased gradually, the current also increased and a sudden rise in the current was observed at a voltage of ~1.8 V, indicating change in its resistance state from initial HRS to some intermediate low resistance state (LRS). As the voltage was kept increasing one more jump in the value of current was observed at a voltage of ~2.2 V and device achieved the resistance state with lowest resistance. This is known as SET process and the device is said to be in the ON state. The occurrence of SET process for more than once, indicated the presence of inherent more than one LRS in the device. Now after the device reached its final LRS, then there was no much increase in current value with the applied voltage. Device maintained the LRS even after decreasing the applied voltage to zero. Now, as the negative voltage was applied to the top electrode, device was still in LRS but as voltage was kept increasing, there was small drop in the current value at −2.3 V and device achieved some intermediate resistance

Please cite this article in press as: Khurana G et al. Multilevel resistive memory switching in graphene sandwiched organic polymer heterostructure. Carbon (2014), http://dx.doi.org/10.1016/j.carbon.2014.04.085

Download English Version:

https://daneshyari.com/en/article/7853645

Download Persian Version:

https://daneshyari.com/article/7853645

Daneshyari.com