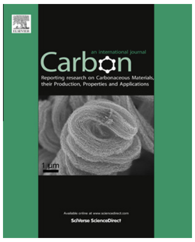
ARTICLE IN PRESS

CARBON XXX (2013) XXX–XXX

Available at www.sciencedirect.com

ScienceDirect

journal homepage: www.elsevier.com/locate/carbon



Suppression of resist contamination during photolithography on carbon nanomaterials by a sacrificial layer

Shih-Wei Lee *, *Matthias Muoth, Thomas Helbling, Moritz Mattmann, Christofer Hierold*

Department of Mechanical and Process Engineering, ETH Zurich, CH-8092 Zurich, Switzerland

A R T I C L E I N F O

Article history:
Received 27 February 2013
Accepted 4 September 2013
Available online xxxx

A B S T R A C T

To suppress photoresist residues on carbon nanotubes (CNTs) resulting from photolithography, CNTs are covered by a sacrificial layer during photolithography. Using aluminum oxide (Al_2O_3) deposited by low temperature atomic layer deposition as the sacrificial layer, the fabricated suspended CNT field-effect transistors exhibit low on-state resistances as low as 91 kΩ and low gate hysteresis of 0.5 V in ambient air. The effectiveness of this technique in suppressing residues on CNTs was affirmed by atomic force microscopy, scanning electron microcopy, and micro Raman spectroscopy. The etchants of Al_2O_3, hydrofluoric acid and phosphoric acid, were found not to cause defects in CNTs while removing the sacrificial Al_2O_3 layer. With the protection of the Al_2O_3 layer, oxygen plasma ashing can be performed without causing further defects in CNTs, and the minimum thickness was determined to be between 9 nm and 17 nm. This simple and effective approach can be easily implemented in different resist-based lithography processes to fabricate carbon nanodevices that are free of resist residues.

1. Introduction

Carbon nano-materials, such as carbon nanotubes (CNTs) and graphene, exhibit outstanding electronic properties, and they are promising candidates for future nano-sensors. The surface cleanliness of carbon nano-materials is essential for good device performances, such as low hysteresis of CNT field-effect transistors (CNTFETs) [1] and low electrical contact resistances [2]. To fabricate nano-sensors with high areal density, photoresist-based photolithography is a common approach for transferring device patterns. However, residues of few nanometers are still remaining after photolithography [1,3–5]. It is difficult to obtain resist-free surfaces once carbon nano-materials have been in contact with photoresists during photolithography. Oxidizing cleaning methods can help to remove the nanoscaled residues, but the selectivity is poor. Stripping photoresists on carbon nano-materials by harsh oxygen plasma ashing will inevitably cause defects in carbon nano-materials [6,7]. Besides plasma cleaning, researchers have also investigated liquid-based cleaning approaches, in an attempt to dissolve undesired residues [1,2,5]. In addition to developing a photoresist removal strategy, particular photoresists, which do not tend to adhere well to carbon nano-materials, have also been investigated [4]. With polymethylmethacrylate (PMMA), a post annealing procedure was reported to further reduce the residues [3,8]. In order to completely avoid the contamination from photoresists, ice lithography has been reported by using an ice film to replace the photoresists in metal lift-off in a scanning electron microscope (SEM) vacuum chamber [9,10].

These approaches are helpful in reducing residues after photolithography, but they are limited either to particular

---

* *Corresponding author*: Fax: +41 446321462.

E-mail address: shlee@micro.mavt.ethz.ch (S.-W. Lee).

0008-6223/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.carbon.2013.09.003

Please cite this article in press as: Lee S-W et al. Suppression of resist contamination during photolithography on carbon nanomaterials by a sacrificial layer. Carbon (2013), http://dx.doi.org/10.1016/j.carbon.2013.09.003

photoresists or to sophisticated equipment, and some of them require additional annealing which can affect (hydrogen-sensitive) contact materials. Instead of cleaning the contaminated surfaces, we first introduced an alternative approach by avoiding contamination from direct contact with photoresists [11]. To prevent carbon nano-materials from coming into direct contact with sticky photoresists, a sacrificial layer is introduced to separate carbon nano-materials from photoresists during photolithography. After processing the photoresists on top of the sacrificial layer, harsh cleaning can be performed as the carbon nano-materials are protected. Eventually, this sacrificial layer can be removed without damaging the carbon nano-materials underneath. This final step also lifts off any remaining photoresist residues. Consequently, the process does not limit the selection of photoresists. Moreover, cleanliness is ensured without high temperature annealing for cleaning.

Here, based on this concept, we selected CNTs as an example to further investigate the effectiveness in maintaining cleanliness during photolithography and the consequential influence on the quality of CNTs while removing the sacrificial layer.

2. Experimental

The material of the sacrificial layer determines the effectiveness of this approach. Here, we chose low temperature atomic layer deposited (ALD) aluminum oxide (Al_2O_3) as the sacrificial layer material for three reasons. First, the Al_2O_3 layer can be etched by hydrofluoric acid (HF) or phosphoric acid (H_3PO_4). HF acid is often used to release CNTs [12,13], and H_3PO_4 acid has not been reported to be harmful for CNTs in the literature. Second, if a silicon dioxide layer (SiO_2) is used as a substrate surface, the Al_2O_3 layer can be selectively removed by H_3PO_4 acid because of the good selectivity over SiO_2 etching [14]. The third reason is that the deposition of Al_2O_3 by ALD is assumed not to cause defects in CNTs because ALD Al_2O_3 has been demonstrated for CNT-device passivation [15–18].

In this section, the effectiveness was first verified by an experiment of stripping resists by a gentle solvent, acetone, and then this approach was applied in the metallization process of the CNT–MEMS integration process [11]. The influence of HF as well as H_3PO_4 on CNTs and the minimum thickness of Al_2O_3 were investigated.

In related work, an ALD layer was patterned as a gate dielectric and a passivation layer for a CNTFET by a similar process [15]. But, in the investigated approach here, the ALD Al_2O_3 layer serves as a sacrificial layer to avoid photoresist contamination during photolithography, and CNTFETs are functional after this layer is completely removed.

2.1. *Photoresist removal with acetone*

To verify the effectiveness of the sacrificial layer in maintaining clean surfaces of CNTs, a photoresist removal test with acetone was performed on as-grown CNTs. First, two identical silicon chips with a silicon nitride (SiN) thin film were used as substrates for the growth of CNTs by catalytic chemical vapor deposition [19]. After the CNT growth, an ALD Al_2O_3 layer of 40 nm was deposited at 150 °C onto the as-grown CNTs on one chip, chip A, and the other chip, chip B without an Al_2O_3 layer, was used as a control sample in this test. Negative photoresist, AZ nLOF 2070, was spun on both chips, followed by a baking step at 110 °C for 60 s. These two chips were subsequently dipped into acetone at 50 °C for 10 min to strip the photoresist. The Al_2O_3 layer on chip A was further etched by buffered hydrofluoric acid (BHF, 6%) for 30 s. To compare the surface conditions of these chips, an atomic force microscope (AFM) was utilized. Fig. 1 shows the AFM height images of these two chips. The surface of chip A, which was covered by Al_2O_3, shown in Fig. 1(a), appears smoother, compared to chip B, shown in Fig. 1(b). The root mean square roughness of chip A is 0.5 nm, which is in good agreement with the roughness of as-deposited LPCVD SiN reported in [20]. Hence, the small grains seen in Fig. 1(a) are assumed to the LPCVD SiN surface roughness. The dots on the CNT and the surroundings shown in Fig. 1(b) are few nanometers in height, and they are likely to be residual photoresists. The particles are similar to those found in literature [1,3–5]. Here, no visible residues were found on the Al_2O_3-covered CNT after stripping photoresists and the Al_2O_3 layer.

2.2. *Metal lift-off with an Al_2O_3 layer*

The method of protecting CNTs by an Al_2O_3 layer during photolithography can be easily incorporated into different processes, such as the CNT–MEMS integration process [11]. Based on the integration process flow, an experimental comparison between two CNT chips processed with and without the Al_2O_3 layer was performed. And the influence of etching acids of the Al_2O_3 layer and the minimum thickness of the Al_2O_3 required to protect CNTs in oxygen plasma ashing were investigated and determined.

2.2.1. *Metallization process*

The process flow of metallization is shown in Fig. 2. An Al_2O_3 layer of 40 nm is globally deposited by ALD at 150 °C to cover as-grown CNTs (Fig. 2(a)). Subsequently, AZ nLOF 2070 is patterned to define metal contact windows by photolithography. With the sacrificial Al_2O_3 layer, oxygen plasma ashing is performed at 100 W for 90 s (Technics Plasma 100-E) to remove residues on the contact windows. The patterned resist layer serves as an etching mask, while the Al_2O_3 layer is etched by 6% BHF for 60 s to make the CNTs accessible to the subsequently deposited metals (Fig. 2(b)). A stack of metals, 2 nm Cr and 200 nm Au, is evaporated and lifted off in a photoresist remover, Methylpyrrolidone (NMP), at 50 °C for 1 h (Fig. 2(c)). The last steps are to etch the Al_2O_3 as well as the SiO_2 in a concentrated HF acid (48%) for 3 min and to dry the chips in a critical point dryer (Fig. 2(d)).

To compare the surface conditions of CNTs with and without an Al_2O_3 layer during photolithography, CNTs were grown on predefined MEMS structures on two Silicon-on-Insulator (SOI) chips, chip C and D. In the following metallization and release steps, these two SOI chips were processed differently. Chip C went through the process flow described above (Fig. 2), and Chip D, used as a control sample, was processed by the same metallization process without an Al_2O_3 layer and without oxygen plasma ashing afterwards. Chip D was released by

Please cite this article in press as: Lee S-W et al. Suppression of resist contamination during photolithography on carbon nanomaterials by a sacrificial layer. Carbon (2013), http://dx.doi.org/10.1016/j.carbon.2013.09.003