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ScienceDirect
Materials Science and Engineering C 27 (2007) 947 – 953
MATERIALS SCIENCE & ENGINEERING C
www.elsevier.com/locate/msec

Templated self-organization of SiGe quantum structures for nanoelectronics

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Received 4 May 2006; received in revised form 7 July 2006; accepted 10 July 2006
Available online 28 November 2006

Abstract

A central challenge for modern device technology aiming towards nanoelectronics, spintronics and quantum computation is to implement exact control in the positioning of nanostructures like quantum dots. Templated self-organization, i.e. combining the well developed top-down approaches to fabricate nanostructures in the microelectronics with bottom-up techniques of self-assembly offers a variety of new paths for the implementation of nanostructures into modern device technology. In this paper two routes are discussed, the ordering of Ge quantum dots on prepatterned Si substrates and the self-scrolling process of Si/SiGe as well as Si/SiGe/Cr hybrid structures into 3-dimensional nano-objects. Prepatterning of Si substrates is achieved by extreme ultra-violet interference lithography (EUV-IL) using diffractive optics exposing areas of typically 0.7×0.7 mm^2 in a single exposure with perfect periodicity. 2-Dimensional hole arrays have been fabricated using EUV-IL and reactive ion etching. Subsequently, molecular beam epitaxy was employed to grow Si/Ge 2-dimensional quantum dot arrays on the prepatterned substrates. Adjusting the exposure and MBE growth conditions, the perfection of ordering and the density of ordered dots is controlled. Moreover, the ordering of quantum dot molecules, comprising 4 quantum dots per lattice point, has been achieved. Scrolled nano-objects were fabricated from Si/SiGe as well as Si/SiGe/Cr hybrid layered structures. Patterned by standard lithographic techniques into mesa structures, underetching leads to a scrolling of the layer stacks into nanotubes, nanospirals and other 3-d objects due to strain relaxation. Entering the nanometer regime anomalous scrolling is observed. Possible applications for quantum dots and scrolled nanotubes for nanoelectronic devices are discussed.

Keywords: Nanoelectronics; Ge quantum dots; Quantum dot crystal; Scrolled heterostructures; Self-assembly; Field effect transistor

1. Introduction

Concepts for future nano-electronic devices frequently involve nanostructures fabricated using the conventional top-down approach of microelectronics, i.e. using advanced lithography and etching techniques [1,2]. Some concepts also make use of self-assembled quantum dots [3,4], however, since those islands grow randomly on the surface with a rather broad size distribution, typically, these devices contain a large number of self-assembled quantum dots. Transferring the advantages of quantum dots and other self-assembled structures into microelectronics [5,6] it is prerequisite to invent technologies which permit addressing of individual nanostructures, in turn this requires the exact positioning of them. To this end a technology called templated self-assembly, combining the top-down approach of microelectronics with the self-assembly of nanostructures is gaining interest [7,8]. In this paper we will discuss to different technologies making use of templated self-assembly for the fabrication of semiconductor nanostructures in the Si–Ge material system. The first technology follows the concept of using prepatterned wafers [7] to order Ge quantum dots on Si substrates. However, here we used extreme ultra-violet interference lithography (EUV-IL) to pattern the wafer. This technology allows exposure of an area of up to 2×2 mm^2 in a single shot [9]. Thus it is suitable for large scale production of ordered arrays of quantum dots.

Interference lithography allows for an excellent precision, and pattern control in the sub-nanometer regime has been achieved using EUV instead of optical beams [10]. Moreover, the method allows the formation of patterns with less than 30 nm periodicity [unpublished results], improving the lateral coupling strength in densely packed Ge dot arrays. Thus, whereas previous studies have been valuable to study the fundamental

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doi:10.1016/j.msec.2006.07.029

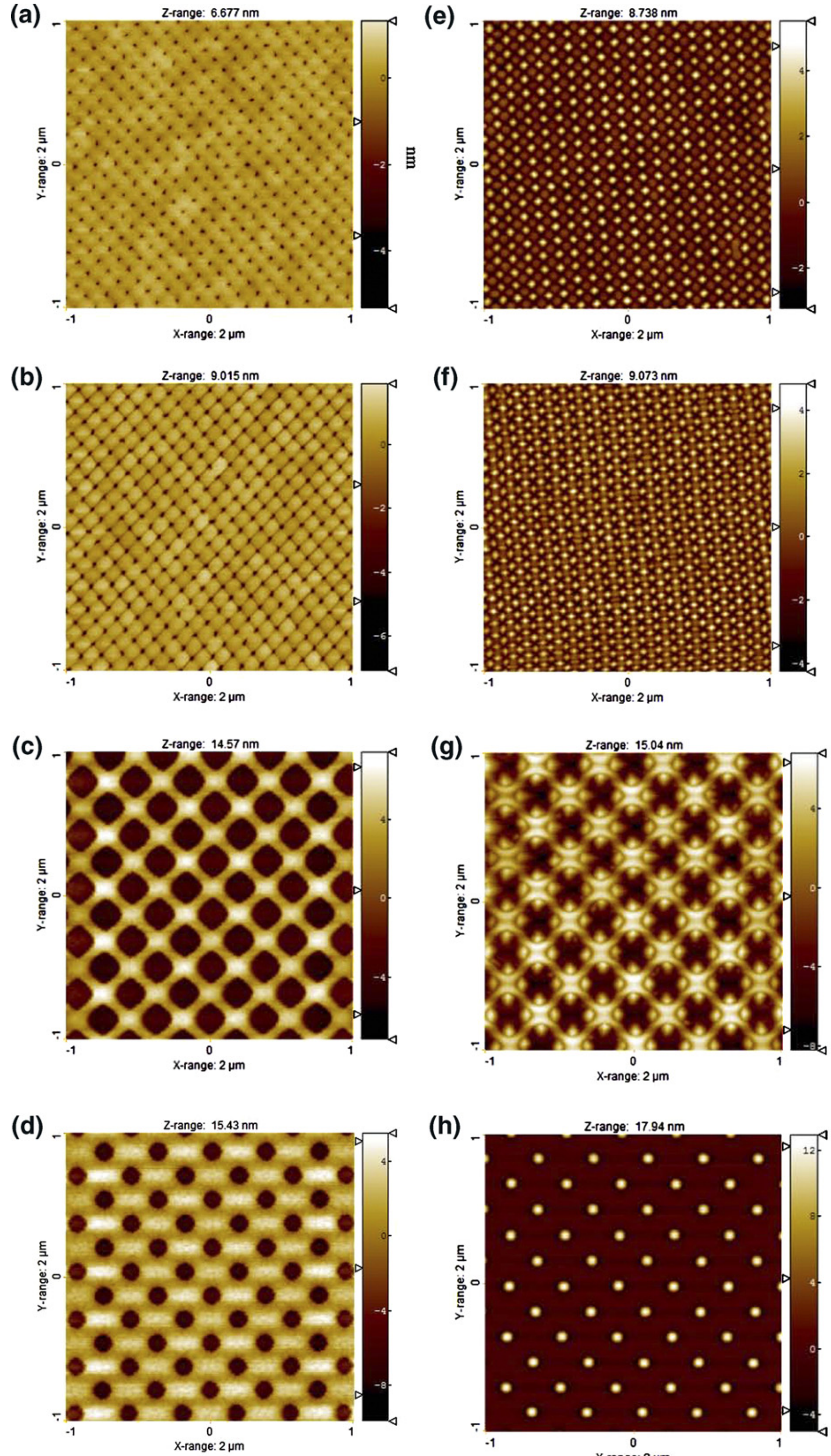

Fig. 1. AFM surface scan of prepatterned Si (100) substrates after deposition of a 50 nm thick Si buffer layer (a,b,c,d) and deposition of a Ge island layer (e,f,g,h).

Fig. 1	a	b	c	d	e	f	g	h
Exposure conditions	55 mJ	75 mJ	90 mJ	450 mJ	55 mJ	75 mJ	90 mJ	450 mJ
Si buffer	50 nm 300 °C	50 nm 300 °C	50 nm 300 °C	50 nm 300 °C	50 nm 300 °C	50 nm 300 °C	50 nm 300 °C	50 nm 300 °C
Ge islands	–	–	–	–	7 ML 460 °C	7 ML 460 °C	7 ML 460 °C	6 ML 500 °C