

Available online at www.sciencedirect.com





Materials Science and Engineering C 27 (2007) 1111-1116

www.elsevier.com/locate/msec

Design and simulation of a nanoelectronic DG MOSFET current source using artificial neural networks

F. Djeffal*, Z. Dibi, M.L. Hafiane, D. Arar

LEA, Department of Electronics, University of Batna 05000, Algeria

Received 4 May 2006; received in revised form 2 September 2006; accepted 4 September 2006 Available online 16 October 2006

Abstract

The double gate (DG) MOSFET has received great attention in recent years owing to the inherent suppression of short channel effects (SCEs), excellent subthreshold slope (*S*), improved drive current (I_{ds}) and transconductance (gm), volume inversion for symmetric devices and excellent scalability. Therefore, simulation tools which can be applied to design nanoscale transistors in the future require new theory and modeling techniques that capture the physics of quantum transport accurately and efficiently. In this sense, this work presents the applicability of the artificial neural networks (ANN) for the design and simulation of a nanoelectronic DG MOSFET current source. The latter is based on the 2D numerical Non-Equilibrium Green's Function (NEGF) simulation of the current–voltage characteristics of an undoped symmetric DG MOSFET. Our results are discussed in order to obtain some new and useful information about the ULSI technology. © 2006 Elsevier B.V. All rights reserved.

Keywords: DG MOSFET; Artificial neural network; Current source; Nanoscale CMOS; Green's function

1. Introduction

The evolution of the semiconductor industry, as predicted by the International Technology Roadmap for Semiconductors (ITRS) [1], shall lead to transistor's minimum feature sizes below 65 nm by the year 2010. Nanoscale sized devices may become an extremely attractive option for development of the integrated circuits with dimensions and performance limits well beyond the ultimate roadmap projections. Among these devices, DG MOSFET presents the most promising device structure. It enables further CMOS scaling beyond the 65 nm technology node (with 25 nm physical gate length). Moreover, it is known for its higher drive current, improved subthreshold slope, improved short channel effect control and potential circuit design flexibility [1-4]. As shown in Fig. 1, with two gates controlling the channel, short-channel effects can be greatly suppressed. Due to the fact that simulation of nanoelectronic circuits has been the primary factor driving improvements in integrated circuit performance and cost, which contributes to the

* Corresponding author. Tel.: +213 73796503; fax: +213 33805494. *E-mail addresses:* faycaldzdz@hotmail.com (F. Djeffal),

zohirdibi@univ-batna.dz (Z. Dibi).

rapid growth of the semiconductor industry, there is a need to develop a new theory and modeling techniques that capture the physics of quantum transport accurately to guide the design for DG MOSFET circuits.

The aggressive scaling scenarios set by the ITRS Roadmap [1] make the accurate simulation of nanoscale MOSFETs a challenging objective of modeling activities. Ballistic transport simulation approaches [5] can account for two-dimensional (2D) quantum mechanical (QM) effects but, by neglecting the effects of scattering, they provide only an upper estimate of the drain current, usually far above the experimental values, so that they are inadequate for device optimization. To extract information accurately about the charge distribution alone require the solution of Schrödinger and Poisson equations based on the NEGF formalism, assuming QM effects are to be fully accounted. But from the circuit modeling point of view even 2D solution of numerical models (NEGF with mode space representation, NEGF with full 2D space representation, Monte Carlo, fully self-consistent coupled Schrödinger and Poisson equations, ...) is an overkill approach in terms of both complexity and computational cost [6-8]. For analytical modeling, in general, it is difficult or almost impossible to obtain closed form analytical models for nanodevices (analytical drain current



Fig. 1. The cross-section view of an *n*-channel fully-depleted SOI double gate MOSFET. The *z*-axis is perpendicular and the *x*-axis is parallel to the channel, respectively.

modeling, physical modeling, ...) [9-11]. Thus, models are obtained by a simplification of the full physical model. The compact models allow for fast system level simulation of the nanoscale circuits. However, the accuracy of such a model can be questionable because of the simplifications made during the model development phase. Model accuracy and simplicity are important for the design of complex systems. Artificial intelligence model would be preferable and could provide practical solutions [12]. We call this type of solution approach as intelligent simulators. In this way, there is a need for designing DG MOSFET circuits. In this sense, this work presents the applicability of artificial neural networks for the simulation of the nanoscale current source for nanoelectronic applications. The database used for the optimization of our neural network is built on the basis of a numerical model of the current-voltage characteristics of a DG MOSFET developed using the Non-Equilibrium Green's Function formalism [5,13,14]. This neural model can be used as the interface between device modeling and circuit simulators like Berkeley SPICE, Cadence Spectre and Anacad's Eldo.

2. Modeling methodology

2.1. Non-Equilibrium Green's Function formalism

The basic structure of the DG MOSFET device used in our study is shown in Fig. 1. As MOSFETs scale to the nanometer regime, canonical carrier transport theories are no longer capable of describing carrier transport accurately. The canonical theories are basically derived from the Boltzmann transport equation (BTE), with more or fewer approximations being made [5]. These models focus on scattering-dominant transport, which typically occurs in long channel devices. However, nanoscale

transistors operate in a quasi-ballistic transport regime [5]. Simulations using conventional models may either under-predict or over-predict the device performance [13,14].

To simulate nanoscale devices, the non-equilibrium Green's function formalism (NEGF) provides one of the best frameworks available [15–17]. The Green's function is solved to obtain the electron density within the device and current at the terminals in the ballistic limit. Under ballistic conditions, the Green's function method is mathematically equivalent to solving the Schrödinger equation with open boundary conditions [18,19]. The resolution of the Schrödinger equation enables us to obtain a set of eigenenergies and eigenfunctions (modes) along the gate confinement direction. The equation that is solved is

$$-\frac{h}{2m_z^*}\frac{\partial}{\partial^2 z}\psi_i(x,z)-qV(x,z)\psi_i(x,z) = E_i(x)\psi_i(x,z) \tag{1}$$

where m_z^* is the electron effective mass in the *z* direction, V(x,z) is the electrostatic potential, and $E_i(x)$ and $\Psi_i(x,z)$ are the eigenenergy and the wave function for mode *i* at slice *x*, respectively. Each vertical slice has a width *a*, all quantities are assumed to be a constant in the *x* direction (Fig. 1). To solve the Green's function (NEGF), a mode space representation is used in the gate confinement direction. This approach greatly reduces the size of the problem and provides good accuracy as compared to full 2D spatial discretization [18,19]. From a computational point of view, the size of the problem is measured by the size of the Hamiltonian. In a full 2D space representation the size of Hamiltonian is defined by the total nodal number in the 2D mesh $(N_x \times N_z)^2$; while in the mode space representation every subband can be treated individually, and the size of Hamiltonian is measured by the nodal number along the channel

Download English Version:

https://daneshyari.com/en/article/7870757

Download Persian Version:

https://daneshyari.com/article/7870757

Daneshyari.com