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Properties of purified direct steam grown silicon thermal oxides

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ABSTRACT

Thermal silicon oxides are known to very effectively passivate silicon surfaces. Choosing a water vapor ambient instead of a dry oxygen atmosphere increases the oxidation rate by about one order of magnitude and considerably reduces process time and costs. State of the art pyrox systems produce steam by pyrolysis of hydrogen and oxygen gas. A new approach is the purification of vaporized deionized (DI) water. In this work we present a direct comparison of both steam generation systems, which are connected to the same quartz tube of an industrial high quality tube furnace. The higher steam saturation of the direct steam process enhances the growth rate by about 20% compared to a pyrolytic steam based process. On low-resistivity p-type substrates, excellent surface recombination velocities of around 25 cm/s are found for both systems after a forming gas anneal. Detailed characterization shows similar physical properties of the oxide layers grown by either steam from pyrolysis or purified steam. Moreover, thermal oxide rear surface passivated silicon solar cells show similar high efficiencies exceeding 18.0% irrespective of the applied steam generation technology.

1. Introduction

The passivation of silicon surfaces by thermal oxides has been a subject of intensive research for many years. Silicon thermal oxide films are regularly grown in an oxygen atmosphere (dry process), which gives excellent interface properties with interface trap densities D_{it} below $4\times10^{9}\,cm^{-2}\,eV^{-1}$ [1] and surface recombination velocities below 15 cm/s on 1 Ω cm floatzone silicon [2].

Recently, we presented several approaches for the implementation of thermal oxide processes for rear surface passivation into industrial cell structures with local rear contacts. Two approaches use a ~10 nm thin oxide layer, upon which we deposit other dielectric layers by means of plasma-enhanced chemical vapor deposition to enhance the optical and electronical properties of the rear surface [3–5]. The use of only a thin oxide layer on the rear surface between the silicon wafer and the aluminum rear contact would lead to a reduced short-circuit current density due to a lower rear surface reflection as was shown by Green [6] and Kray et al. [7]. In addition, the use of capping layers on top of the thin thermal oxide layer can improve the electronic properties of the silicon–insulator interface [8–11]. Another approach uses a thick oxide layer [12,13], as investigated in this paper. The oxide layer thickness on the rear surface decreases during processing to a final thickness of around 100 nm in the solar cell device [13], which already allows for an average internal rear surface reflection of 94% in combination with an evaporated aluminum layer [7].

Nevertheless, with increasing oxide film thickness, the oxide growth rate decreases, which prolongs the duration of dry oxidation processes to several hours, when growing oxide layers thicker than 100 nm. Using water vapor (wet oxidation) instead of oxygen as an oxidant increases the oxide growth rate by up to one magnitude [14,15] due to a higher solid solubility of steam in the silicon oxide, which makes wet oxidation interesting for processes, where thicker oxide layers are required. In addition, the thermal stress to the wafers is reduced, compared to the use of a dry oxygen ambient [16], due to the incorporation of hydroxyl groups. However, wet oxidation does not fully reach the surface passivation quality of dry processes [16,17]. State of the art systems generate steam in a pyrolytic torch, using high purity hydrogen and oxygen gas. An alternative approach uses vaporized and consecutively purified deionized water [18], which reduces the cost [19] and improves the safety due to the elimination of hydrogen and oxygen gas from the facility.

Benick et al. [20] showed that for high efficiency solar cells, both purified steam and pyrolysis yield similar high open circuit voltages. However, the two steam generation systems were connected to different oxidation tubes and no detailed information on the properties of the oxide layers and the interface were presented.

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In this paper we present a direct comparison of both steam generation technologies with both systems connected to the same quartz tube. In addition to previous work [21] this work includes a comprehensive characterization of the oxide layers and the Si–SiO_2 interface as well as a comparison on device level. For the sample and solar cell preparation, we use industrial production equipment [22].

2. Experimental

2.1. Sample preparation

We use 250 μm thick, 125 mm large (pseudo-square), shiny-etched floatzone (FZ) p-type wafers with a base resistivity of 1 Ω cm to characterize the oxide layer and the interface. Possible surface contaminations [23] are removed in a first step by wet chemical cleaning in a high capacity automated industrial type wet bench using carriers holding up to 100 wafers. A chemical oxide grows on the surface of submersed wafers in a heated oxidizing solution of NH_4OH, H_2O and H_2O_2. A dip in diluted HF solution then removes the chemical oxide. A second cleaning step consists of an $HCl/H_2O/H_2O_2$ mixture, also followed by an HF dip. After rinsing in DI water, a steady flow of heated air then dries carrier and wafers in the same system.

The thermal oxide is grown in a quartz tube, located in an automated horizontal industrial tube furnace, with quartz boats holding up to 212 wafers. Loading of the wafers is done while purging with N_2. The ramp up in an atmosphere containing oxygen in low concentration results in the growth of an initial thermal oxide layer of 5 nm thickness. At the oxidation temperature of 950 °C, the system switches to water vapor supply. A post-oxidation anneal at the same temperature in an N_2 ambient follows, before ramping down to 850 °C and unloading the wafers.

Two different steam generation systems, both connected to the same tube, provide water vapor for oxidation: the first is a conventional pyrox system that produces steam by pyrolytic generation of high purity O_2 and H_2 gas at a temperature above 700 °C. For safety reasons, oxygen is added to the gas stream in an overstoichiometric ratio $H_2{:}O_2 = 2{:}1.25$ (by mole fraction). A second system, connected to the same oxidation tube, uses DI water as a direct steam source (in the following denoted "steamer"). This system uses a non-porous hydrophilic membrane to purify evaporated DI water. The membrane restricts access to the oxidation tube to water molecules and removes dissolved gases, metal impurities and particles from the steam [18]. Earlier experiments used nitrogen bubbled into hot deionized water [16], thus requiring a carrier gas. In contrast to this approach, the steamer system does not need a carrier gas, resulting in a 100% steam saturated atmosphere, which increases the oxide growth rate. We account for the higher oxidation rate by reducing the oxidation plateau time from 20 min for the use of the conventional pyrox system to 18 min when using the steamer system. Apart from that, we leave all other process parameters unchanged.

We use the pyrox system as steam source in the first oxidation, and the steamer for the second process. The comparability of the results is ensured by using wafers that are cleaned in the same batch and using the same quartz tube in two consecutive oxidations. Annealing the samples in forming gas (FGA) for 25 min at 425 °C improves the surface passivation quality. Characterization of the samples takes place both before and after a FGA with the techniques mentioned below.

2.2. Characterization

The quasi steady state photoconductance (QSSPC) method [24] enables the determination of the effective minority carrier lifetime τ_{eff} at an injection density of $\Delta n = 5 \times 10^{14}\ cm^{-3}$, representing low level injection conditions. The surface recombination velocity

$$S = \frac{W}{2}\left[\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)^{-1} - \frac{1}{D}\left(\frac{W}{\pi}\right)^2\right]^{-1} \quad (1)$$

then follows from τ_{eff} according to [25] using the sample thickness $W = 250\ \mu m$, the intrinsic recombination limited bulk lifetime $\tau_{bulk} = 2$ ms [26] and the diffusion constant $D = 27.0$ cm/s.

Capacitance–voltage (*CV*)-measurements enable a further characterization of the silicon–silicon oxide interface. Nine individual positions are tested on each sample using simultaneous measurement of a quasi static and a high-frequency pulsed *CV* curve with a pulse length of $\tau_p = 10^{-4}$ s. Contacting and measuring of the sample is done using a mercury probe with a dot size of $0.0135\ cm^2$. For all measurements bias light is switched on to facilitate the generation of electron–hole–pairs. This approach enables the extraction of the midgap interface trap density D_{it} and the total charge density Q_{tot} from the *CV* data with equations published by Schroder [27].

We use a Woollam M-2000 spectral ellipsometer for the optical characterization of the oxide layers. After three measurements, thereby varying the angle of incidence between 65° and 75°, the fitting of the Tauc–Lorenz-model to the ellipsometry data enables the extraction the film thickness, the refractive index *n*, and the extinction coefficient *k* of the films. For each set of wafers, three samples are measured.

For Fourier transform infrared spectroscopy (FTIR) measurements, a Bruker IFS 113-V with normal incidence is used. The measurement covers wavenumbers from 400 to 4000 cm^{-1}. A reference sample of the same silicon material but without silicon oxide layers present at the surfaces permits the determination of the absorbance spectrum for the silicon bulk. This signal is subtracted from the absorbance spectra measured for the samples yielding the sole absorbance of the oxide films. Finally, a base line correction facilitates the evaluation of individual peaks.

2.3. Solar cell fabrication

The fabrication of rear surface passivated solar cells allows for a comparison of both systems in a working device. Fig. 1 schematically illustrates the device structure. For device fabrication we use 125 mm (pseudo-square) sized, boron-doped Czochralski (Cz) silicon wafers with a resistivity of ~2.7 Ω cm. The final cell thickness is ~110 μm, which makes the cell more sensitive to rear surface passivation [7,28]. The front surface of the cells features a random pyramid texture and a phosphorus diffused emitter with a sheet resistance of 75 Ω/sq. A SiN_X layer, deposited by plasma-enhanced chemical vapor deposition, serves as an

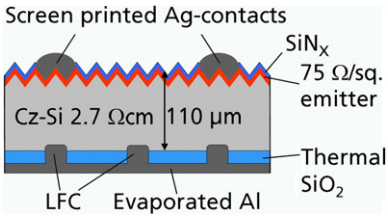

Fig. 1. Schematic of the fabricated device. The rear surface passivation consists of a 100 nm thick layer of thermal oxide.