Cadmium ion soaking treatment for solution processed $CuInS_xSe_{2-x}$ solar cells and its effect on defect properties

Bao Lei, William W. Hou, Sheng-Han Li, Wenbing Yang, Choong-Heui Chung, Yang Yang *

Department of Materials Science and Engineering, University of California, Los Angeles, 420 Westwood Plaza, Los Angeles, CA 90024, USA

ABSTRACT

Recombination of charge carriers due to electronically active material defects is one of the major factors limiting power conversion efficiency in solar cells. We have studied the defect behavior in $CuInS_xSe_{2-x}$ solar cells fabricated through a solution process with a maximum heating temperature of 390 °C. By introducing a cadmium ion soaking step into the fabrication process, we find that the recombination rate can be reduced. Through the use of capacitance–voltage (C–V) profiling, drive level capacitance profiling (DLCP) and admittance spectroscopy analysis, the cadmium ion soaking process was found to increase the charge carrier concentration in the bulk of the absorber, and shift the energy level of the N1 defect toward the valence band edge. The soaking process was found to most obviously affect the open circuit voltage with an average improvement of 33 mV.

Published by Elsevier B.V.

1. Introduction

$CuInS_xSe_{2-x}$ (CISS) and other chalcopyrite-based solar cells have received substantial research interest due to their excellent light absorption, relatively low cost and outstanding performance compared to other thin-film solar cells [1–3]. While the most efficient $CuIn_xGa_{1-x}Se_2$ (CIGS) solar cells based on vacuum evaporation or sputtering of absorber materials have approached 20% power conversion efficiency, alternative solution-based absorber deposition approaches have also attracted attention [4], due to their potentials for further reducing production costs. Examples include electrochemical deposition [5,6], nanoparticles-precursor deposition [7,8], and spray pyrolysis [9].

Recently a hydrazine-based solution process has been demonstrated for the deposition of several chalcopyrite materials [10–12], and its applications in solar cell fabrication have been explored [13–17]. This process is advantageous due to its low processing temperature, facile compositional control, and better material utilization rate. Additionally, in contrast to some other solution-based methods, it avoids the need for selenization procedures and limits the introduction of organic impurities into the resulting films. A 7.4% power conversion efficiency has already been demonstrated based on a CISS absorber layer fabricated at an annealing temperature of 350 °C [17].

To further improve the device performance, it is essential to understand the more detailed defect physics and recombination mechanisms. Various techniques, including admittance spectroscopy (AS) [18,19], deep level transient spectroscopy (DLTS) [19], and drive level capacitance profiling (DLCP) [20] have been widely employed in the analysis of vacuum processed CISS/CIGS solar cells to examine the energetic and spatial distribution of defects in the absorber layer. A defect state at 0.3 eV above the valence band edge, known as N2, is commonly reported [19], and is typically attributed to the In_{Cu} point defect [21]. Another defect, known as N1, has been observed, and has been shown to produce energy levels between 0.1 and 0.3 eV from the valence band edge [20]. The nature of the N1 defect is still unknown, with possible sources ranging from defects formed at the CIGS/CdS interface [19], inside the CIGS bulk [22], or at the CIGS/Mo interface [23]. This defect may also have an entirely different origin and structure based on differences in the fabrication and processing techniques used to produce each device.

In this work, we report that by introducing an additional Cd ion solution soaking step into our device fabrication process, the open circuit voltage (V_{oc}) can be improved, possibly as a result of reduced recombination losses. Using C–V, DLCP profiling and admittance spectroscopy, we have found that the effects of this process on device performance can be correlated with changes in charge carrier densities and defect energy levels.

2. Experimental details

2.1. Device fabrication

The devices consisted of a soda lime glass substrate with a 1 μm thick sputtered Mo layer for the bottom electrode, followed by a CISS film deposited through the hydrazine solution process.

* Corresponding author.
  E-mail address: yangy@ucla.edu (Y. Yang).
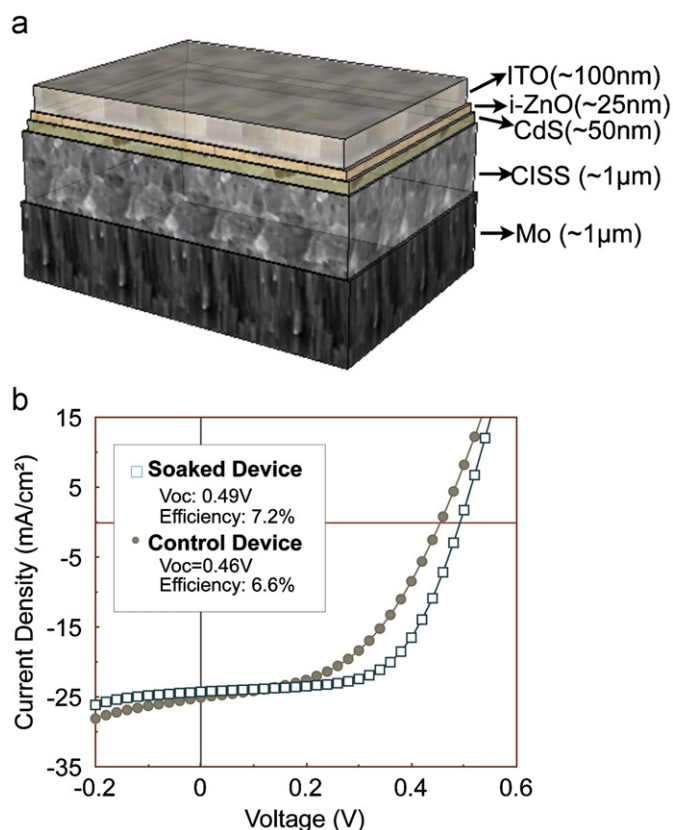 *URL:* http://yylab.seas.ucla.edu (Y. Yang).

Fig. 1. (a) Structure of our CISS solar cell devices. (b) *J–V* curves of the devices with and without Cd soaking process.

A cadmium sulfide (CdS) layer was then deposited via chemical bath deposition, followed by an intrinsic zinc oxide (ZnO) layer and an indium tin oxide (ITO) layer, both deposited via sputtering. The device area was 0.12 cm^2. The structure of the device is illustrated in Fig. 1(a).

The solution deposition of CISS films was achieved through the repeated spin-casting of a precursor solution. The precursor solution was prepared by mixing the Cu_2S solution (1 mmol Cu_2S and 2 mmol S in 2 mL hydrazine) and In_2Se_3 solution (1 mmol In_2Se_3 and 1 mmol Se in 4 mL hydrazine). The precursor film, deposited by spin-casting from the precursor solution, was annealed at a maximum temperature of 390 °C for 30 min in order to convert it to the CISS phase, as discussed in our earlier works [17,24]. The final film thickness was between 1 and 1.2 µm. All of the processes discussed above were performed under a nitrogen environment with O_2 and H_2O levels below 1 part per million (ppm).

The chemical bath deposition of CdS was performed using an aqueous solution containing cadmium acetate ($Cd(OAc)_2$), thiourea, ammonium hydroxide ($NH_3 \cdot H_2O$) and ammonium acetate (NH_4OAc). The reaction was maintained at 65 °C throughout the deposition. The deposition time was adjusted between 20 and 22 min to yield a 25 nm CdS film.

In this study we introduced a unique step after the final annealing of CISS and before the chemical bath deposition of CdS, which was to soak the finished CISS films in a $Cd(OAc)_2$ aqueous solution at 65 °C for 1 hour. The concentration of the $Cd(OAc)_2$ solution used for soaking was about 0.27 mM. Ten control devices without this step were fabricated, and compared to 10 devices fabricated with the soaking process included.

The cadmium soaking process is similar to the cadmium partial electrolyte treatment (CdPE) studied previously by several groups [25,26]. A major difference is that in a typical CdPE process, ZnO is sputtered right after the soaking of CIGS/CISS

films in solutions with Cd ions. In our experiments, however, standard CdS deposition is performed after the extra Cd ion soaking and before the ZnO deposition. In this way we can exclude the effect of sulfur as well as the buffer role of the CdS layer, and focus our analysis on the effects of the amount of cadmium incorporation.

2.2. Device characterization

The current density–voltage (*J–V*) characteristics of the photovoltaic devices were measured using a Keithley 2400 source meter. Illumination was provided by a Newport Oriel solar simulator (Model 91191-1000) with an AM1.5G filter (Model 81088). The light intensity was stabilized at 100 mW/cm^2 using a Newport Oriel 68945 light intensity controller [27].

The capacitance of the photovoltaic device was measured using a Hewlett-Packard 4284A LCR Meter. Electrical contact to the devices during LCR measurements was provided by a Janis cryogenic probe station with an attached Lakeshore 331 temperature controller. The temperature was monitored using a thermocouple placed in contact with the sample location.

3. Results

3.1. I–V characteristics

Fig. 1(b) shows the current density–voltage (*J–V*) characteristic curves for devices with and without the $Cd(OAc)_2$ soaking treatment. The devices with Cd soaking typically achieved higher power conversion efficiencies (7.2%) compared to the ones without (6.6%). The improvement is mainly due to an increase in Voc from 0.46 to 0.49 V.

We analyzed the *J–V* curves of the devices measured under dark using the one diode model. By fitting the dark *I–V* curves to equation [28]:

$$J = J_0 \left[\exp \left(\frac{V - J \times R_s}{nkT} \right) - 1 \right] + \frac{V - J \times R_s}{R_{sh}}$$

We obtained the area specific series resistance (R_s), shunt resistance (R_{sh}), and the diode ideality factor (n) as well as the reverse saturation current density (J_0). R_s was calculated by comparing the light and dark *I–V* curves [29,30]. Compared to extracting the R_s directly from the slope of the *J–V* curve at high voltage points, this method also takes into account the lateral resistance of the transparent conductive oxide, and therefore provides a more accurate estimation of R_s [29–31]. R_{sh} was calculated according to the slope of the dark *I–V* curves near the zero voltage point. J_0 and n were extracted from the slope and intersect of the log(*J*)–V curves in the linear ranges.

Fig. 2 shows the comparison of each parameter obtained from the light and dark *J–V* curves, with 10 samples in each group. Standard statistical tests confirm that the increase of Voc in the Cd ion treated samples is significant. The averaged Voc improved from 0.458 ± 0.011 to 0.491 ± 0.004 V as a result of the soaking treatment. However, the average short circuit current (Jsc) of the treated samples was somewhat reduced. We expect that this is due to changes in the optical scattering effect at the surface of the CISS layer, rather than the recombination of photo-generated carriers, since the Voc did not decrease as well. The fill factor also showed improvement, possibly as a result of the improved R_s and J_0. The drop of Jsc made the improvement on efficiency less statistically significant, as the variation of efficiencies is close to the average increase (about 0.4%).

Among the dark *I–V* fitting parameters, we noticed a decrease in J_0. According to the fundamentals of diode theory, both J_0 and