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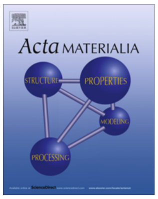

Carbon out-diffusion mechanism for direct graphene growth on a silicon surface

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ABSTRACT

Direct growth of graphene on silicon (Si) through chemical vapor deposition has predominantly focused on surface-mediated processes due to the low carbon (C) solubility in Si. However, a considerable quantity of C atoms was incorporated in Si and formed $Si_{1-x}C_x$ alloy with a reduced lattice dimension even in the initial stage of direct graphene growth. Subsequent high temperature annealing promoted active C out-diffusion, resulting in the formation of a graphitic layer on the Si surface. Furthermore, the significantly low thermal conductivity of the $Si_{1-x}C_x$ alloy shows that the incorporated C atoms affect the properties of a semiconductor adjacent to the graphene. These findings provide a key guideline for controlling desirable properties of graphene and designing hybrid semiconductor/graphene architectures for various applications.

1. Introduction

There is increasing interest in direct graphene growth on targeted semiconductor substrates because the unique properties of graphene-semiconductor interfaces result in synergetic effects in hybrid device applications [1–6]. In particular, combination of graphene with silicon (Si) has been intensely studied for a wide range of applications because of the natural abundance of Si and its CMOS compatibility [7,8]. However, the mechanism of direct graphene growth on Si has not been fully elucidated in spite of widespread interest. Recent studies of graphene growth on Si have mainly focused on the surface-limited reaction process due to the low carbon (C) solubility in bulk Si (3×10^{17} atoms/cm^3 at the melting point) [9,10]. However, theoretical and experimental studies have demonstrated that not only does C have a high diffusivity in Si [11,12], but it also contributes to the build-up of a narrow C-containing layer near the Si surface, even at temperatures lower than 1000 °C [13,14]. Furthermore, the equilibrium C solubility near the Si surface is up to 10^4 times greater than that in bulk Si for low diffusion energy barriers. In addition, C atoms incorporated into Si are another source of graphene or unintentional impurities in Si during the high-temperature growth process. Thus, a precise mechanism for graphene growth would assist with the fabrication of well-defined hybrid architectures with desirable properties.

In this work, the mechanism of direct graphene growth on Si was investigated using a conventional chemical vapor deposition (CVD) process. Single crystalline Si nanowires (SiNWs) and a flat Si wafer were used as the growth substrates for the graphene layer to systematically analyze their atomic behaviors. The structural transition from Si to $Si_{1-x}C_x$ NWs revealed the rapid incorporation of substitutional carbon in Si during graphene growth. In addition, the appearance of graphene on the Si surface after thermal annealing of $Si_{1-x}C_x$ NWs indicates that surface segregation of the incorporated C atoms plays a dominant role in direct graphene growth on Si. Systematic measurement of the thermal conductivity of the $Si_{1-x}C_x$ NWs supported this understanding of the growth mechanism and illustrated the significant influence of C incorporation on the performance of semiconductor/graphene hybrid structure applications.

2. Experimental

2.1. Two-step process for direct graphene growth on Si

The synthesis of graphene on SiNWs was achieved as follows. First, 300 nm SiO_2/Si substrates (or quartz plates), which had a

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thermally deposited 3 nm gold (Au) thin film layer, were loaded in a homemade CVD system and placed in the center of a quartz tube furnace. Au-catalyzed SiNW growth was performed in the temperature range of 480–520 °C using silane (SiH_4) gas with a flow rate of 40 standard cubic centimeters per minute (sccm). Subsequently, the substrates were moved to the cooling zone and cooled to room temperature under H_2 flowing at a rate of 50 sccm. Then, the furnace was heated to 900–1000 °C, followed by annealing for 10 min to remove unwanted contamination from the quartz tube. Direct graphene growth was achieved by introducing 40 sccm methane (CH_4, 100%) gas into the chamber at a total pressure of ~10 Torr. The growth time was varied from 2 to 20 min in order to investigate the influence of C incorporation during direct graphene growth. A post-annealing process was carried out under a hydrogen (H_2, 50% diluted in Ar) atmosphere at the same temperature for 15 min.

2.2. Characterization

For field emission scanning electron microscopy (FESEM), transmission electron microscopy (TEM), and selected area electron diffraction (SAED) studies, as-grown NWs were separated from the substrates in an ultrasonic ethanol bath and were dropped onto a copper grid without a supporting film. High-resolution TEM lattice and SAED measurements were carried out on a JEM-2100F TEM operated at a 300 kV accelerating voltage. Raman spectroscopy (WITEC) at an excitation energy of 2.33 eV (532 nm excitation laser) and a Fourier-transform infrared (FTIR) spectrometer (Bruker, IFS 66 v/s) were used to characterize the SiNWs after direct graphene growth. The absorption of all samples was computed with baseline and substrate subtraction after normalization. To minimize the effect of the substrate on Raman and FTIR analyses, an aluminum (Al) film was thermally deposited on the slide glasses with a thickness of 200 nm. The crystal structures of NWs on quartz plates were characterized using X-ray diffraction (XRD, Rigaku D/max-rc) in a 2θ range of 20–100°.

2.3. Measurement of thermal conductivity

The micro-device used to measure the thermal conductivity of NWs was composed of heating and sensing membranes. A platinum (Pt) coil, which was used as the heater and sensor, was deposited onto the Si nitride beams. In order to prevent heat conduction through the substrate, suspended membranes were fabricated through the etching of a Si substrate using a tetramethylammonium hydroxide (TMAH) solution. NWs were loaded onto the micro-devices using a solution drop-dry method, and the suspended structure was placed in a cryostat at a vacuum level higher than 9×10^{-6} Torr. For Pt deposition, we used a focused ion beam (FIB)/SEM dual-beam system (FEI, Helios 400S). During Pt deposition, we used 'SEM deposition mode' in which an electron beam was used (10 keV, 15–20 s) to minimize nanowire damage.

3. Results and discussion

Fig. 1a shows a controlled two-step process for direct growth of a graphene layer on SiNWs. Highly dense Au-catalyzed SiNWs were synthesized [15–17], and, to prevent native oxide formation on SiNWs, direct graphene growth was subsequently carried out at 1000 °C. The FESEM and TEM images in Fig. 1b and c show that the overall morphology of the SiNWs is retained after direct graphene growth at high temperature. The relatively large D peak (~1300 cm^{-1}) and weak 2D peak (~2700 cm^{-1}) in Fig. 1d indicate the nanocrystalline nature of the directly-grown graphene, which has been commonly observed [9,18,19]. Au clusters formed during NW growth unintentionally affect direct graphene growth, but the presence of graphene on the NW surface (without Au clusters) and on the Si wafer was confirmed using Raman and TEM measurements.

To systematically investigate the initial stages of graphene growth on SiNWs, we grew the graphene layers at different growth times (T_G): 2, 5, 10, and 20 min. Fig. 2a presents the Raman spectra of the NWs with the corresponding T_G. Positions and integrated intensities of Raman peaks were measured using Lorentzian fitting after subtracting the strong Si spectrum. It is known that vibration of a C local mode at ~605 cm^{-1} determines the presence of substitutional carbon in the Si structure [20,21]. Although a distinct change in peak position was not observed with T_G, the increase in integrated intensity ratio (I_C to I_{Si}) indicates that C atoms diffused into the Si lattice and occupied substitutional sites (inset of Fig. 2a and Supplementary Fig. S1) [22,23]. The presence of a Si–C peak at $T_G = 2$ min indicates that C atoms rapidly diffuse into Si

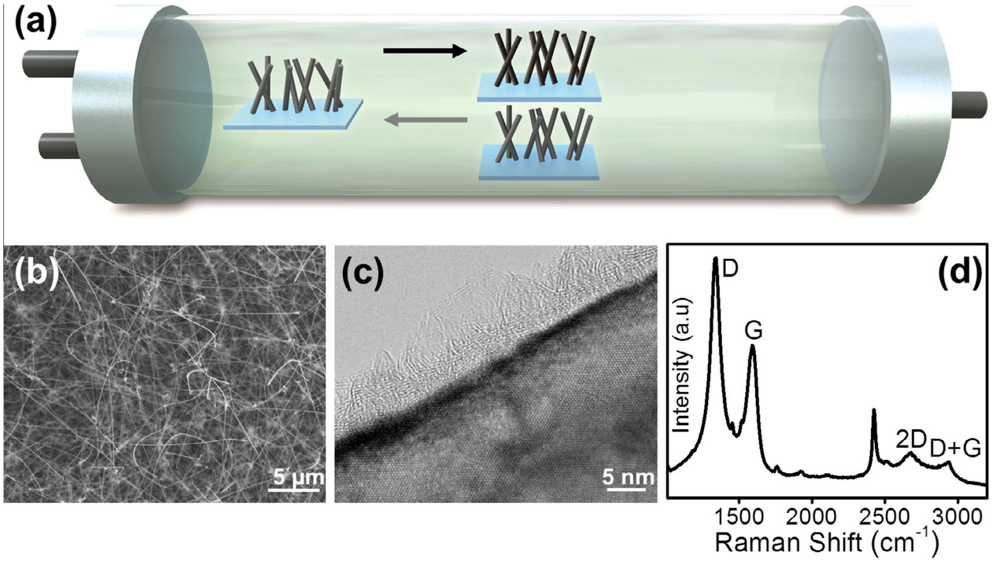

Fig. 1. (a) Schematic of direct graphene growth on highly dense SiNWs using a two-step process. (b) SEM and (c) TEM images and (d) Raman spectra of multilayered graphene grown on SiNWs.