Available online at www.sciencedirect.com

ScienceDirect

Acta Materialia 64 (2014) 62–71

Acta MATERIALIA

www.elsevier.com/locate/actamat

Control of surface morphology and crystal structure of silicon nanowires and their coherent phonon transport characteristics

Seung-Yong Lee [b,c,1], Gil-Sung Kim [b,1], Jongwoo Lim [d,e], Seungwoo Han [f], Baowen Li [c], John T.L. Thong [g], Young-Gui Yoon [a], Sang-Kwon Lee [a,*]

[a] Department of Physics, Chung-Ang University, Seoul 156-756, Republic of Korea
[b] Department of Semiconductor Science and Technology, Semiconductor Physics Research Center (SPRC), Chonbuk National University, Jeonju 561-756, Republic of Korea
[c] Department of Physics, National University of Singapore, Singapore 117542, Republic of Singapore
[d] Department of Chemistry, University of California, Berkeley, CA 94720, USA
[e] Materials Science Division, Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA
[f] Department of Nano Mechanics, Korea Institute of Machinery & Materials (KIMM), Daejeon 305-343, Republic of Korea
[g] Center for Integrated Circuit Failure Analysis and Reliability (CICFAR), Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576, Republic of Singapore

Received 21 October 2013; received in revised form 13 November 2013; accepted 14 November 2013
Available online 18 December 2013

Abstract

We report on the first experimental observation of coherent phonon transport characteristics in silicon nanowires (SiNWs) synthesized by a one-step surface reconstruction growth mechanism. As-grown SiNWs taper down along the growth direction alongside a decrease in both roughness and stacking fault density. Furthermore, by systematically measuring the temperature-dependent thermal conductivity using a conventional thermal bridge method, we found that the measured thermal conductivity values of surface-reconstructed (SR)-SiNWs (13–20 $W\,m^{-1}\,K^{-1}$) at room temperature are markedly lower than that predicted from the conventional diffuse phonon transport model for given NW diameters. We also observed that the thermal conductivities of SR-SiNWs exhibit an unexpected power law of $\sim T^{\alpha}$ ($1.6 \leqslant \alpha \leqslant 1.9$) in the temperature range of 25–60 K, which cannot be explained by the typical Debye $\sim T^{3}$ behavior. Interestingly, our experimental results are consistent with a frequency-dependent model, which can be induced by coherence in the diffuse reflection and backscattering of phonons at the rough surface and stacking faults on SR-SiNWs, resulting in the suppressed thermal conductivity. Therefore, the demonstrated rational synthesis model and measurement technique promise great potential for improving the performance of a wide range of one-dimensional NW-based thermoelectric devices.

Keywords: Silicon nanowires; Thermal conductivity; Stacking fault; Phonon boundary scattering; Coherent phonon transport

1. Introduction

Over the past few years, a number of research groups have intensively studied, both experimentally [1–5] and theoretically [6–10], the enhancement of thermal properties (figure-of-merit; ZT) of silicon nanowires (SiNWs), primarily focusing on diameter reduction and surface roughness. Of particular importance in the application of SiNWs to thermoelectric (TE) devices [11,12] is the need to reduce the effective thermal conductivity of the NW through enhancement of phonon-boundary scattering at rough surfaces and/or interlayers, which can act as important phonon scattering interfaces. Control over the surface morphology (roughness and facets), crystal structure and crystalline defects in SiNWs can provide a route to the reduction of thermal conductivity via diffuse reflection

* Corresponding author.
E-mail address: sangkwonlee@cau.ac.kr (S.-K. Lee).
[1] These authors contributed equally to this work.

1359-6454/$36.00
http://dx.doi.org/10.1016/j.actamat.2013.11.042

and backscattering. The Yang and Majumdar [1,3,4] research groups have used metal-catalyzed vapor–liquid–solid (VLS) growth and the wet chemical etching process to show that the thermal properties of thin and rough SiNWs can be improved 100-fold relative to that of bulk Si. More recently, Sansoz [10] showed by molecular dynamics (MD) simulations that the thermal conductivity is greatly reduced in crystalline ⟨1 1 1⟩ SiNWs having periodic sawtooth faceting compared to those for smooth SiNWs with the same dimensions, thus providing a strategy to optimize the design and performance of SiNWs as TE elements.

To date, several research groups have documented faceting on SiNW sidewalls in the VLS growth process. Recently, Hannon et al. [13] observed nanoscale faceting in SiNWs during Au-catalyzed VLS growth in ultra-high vacuum, and reported that facets on the SiNW sidewalls were created by the interplay of Au diffusion from Au–Si droplets and a subsequent vapor–solid (VS) process with increasing growth time. den Hertog et al. [14] also reported that diffusion of Au in SiNWs could be controlled by silane partial pressure and growth temperature. More recently, Oehler et al. [15] found that the presence of Au on SiNW sidewalls has a critical effect on its morphology because Au diffusion along the sidewalls causes surface reconstruction, which in turn leads to faceting.

However, there have been no systematic studies on the formation, and the resulting phonon transport characteristics, of ⟨1 1 1⟩-oriented stacking faults on/in {1 1 1}/{1 0 0} SiNW sidewalls facets. In order to enhance phonon scattering in SiNWs, we report in this study a strategy to control the surface morphology and crystal structure of SiNWs by Au-induced VLS–VS growth at a low silane partial pressure. We have observed that surface-reconstructed SiNWs (SR-SiNWs) have not only a rough surface morphology on the sidewalls with {1 1 1}/{1 0 0} faceting, but also stacking faults inside the SiNWs. Moreover, to further elucidate the effects of roughness- and stacking-fault-induced phonon-boundary scattering on coherent phonon transport characteristics in SR-SiNWs, we present systematic experimental studies in terms of roughness, facets and stacking faults using a conventional thermal bridge method over a temperature range of 25–300 K.

2. Experimental

2.1. Synthesis and characterization of SR-SiNWs

The SiNWs were synthesized by an Au-catalyzed hot-wall chemical vapor deposition (CVD) growth mechanism in a quartz-tube thermal furnace with SiH_4 (3% diluted in Ar) as a Si source at a base pressure of 2×10^{-2} torr. Prior to Au-catalyst deposition, a Si wafer was cleaned by buffered hydrofluoric acid (BHF). Au catalyst (~2 nm in thickness) was deposited by e-beam evaporation onto the Si wafer. Then, the Au-coated Si substrates, which have been singulated into 0.7 cm × 0.7 cm dies, were placed into a quartz-tube furnace. The growth experiments were carried out at a pressure of ~3 torr (partial silane pressure of $\sim 8.2 \times 10^{-3}$ torr), a temperature of 550 °C and a SiH_4 flow rate of 3 sccm. The detailed experimental steps are described in our published reports [16,17]. The dimensions, surface morphology, crystal structures and composition of as-synthesized SiNWs were characterized using high resolution scanning electron microscopy (SEM), transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) with energy dispersive X-ray (EDX) analysis. The cross-sectional and longitudinal-sectional specimens for the TEM analysis were prepared using standard procedures in a dual beam focused ion beam (FIB) machine (see details in Fig. S.1 in Supplementary material).

2.2. Microdevice chip, NW manipulation and measurement setup for thermal property measurements

To measure the thermal properties of SiNWs, we used a suspended microdevice chip fabricated by a standard microelectromechanical systems (MEMS) process, as shown in Fig. 1. The fabricated microdevice chip has heating and sensing regions, which were formed by platinum (Pt) coils on silicon nitride (SiN_x) membranes. The local temperature of each membrane can be estimated by measuring the temperature-dependent resistance of the Pt coil. For the placing of a single SiNW between two suspended membranes, a micromanipulator with a tungsten tip was used under an optical microscope. First, as-synthesized SiNWs were rubbed onto a TEM grid, and the tungsten tip was moved near a desired single SiNW on the TEM grid. As a result, the SiNW was naturally attached to the end of the tungsten tip by electrostatic force. Thereafter, we could easily place the SiNW onto the suspended microdevice chip. Additionally, Pt/C composite was also deposited using an e-beam induced deposition (EBID) on the contact regions to reduce the contact thermal resistance between the SiNW and metal electrodes, as shown in Figs. 1 and S.2. The detailed system set-up and procedure for measuring the thermal conductivity of SiNWs are well documented in the literature [1–3,18]. Fig. 2a and b shows the schematic measurement setup of the suspended SiNW

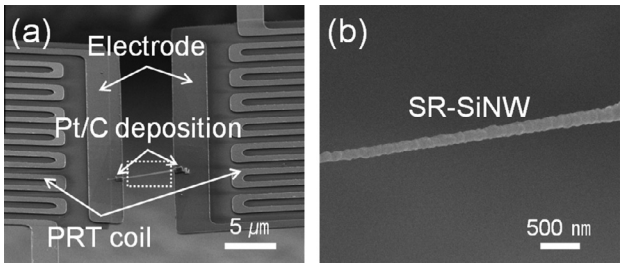

Fig. 1. Microchip for thermal conductance measurement. (a) SEM image of SR-SiNWs placed onto a microdevice chip with Pt/C composite thermal contact by EBID in FIB. (b) Enlarged SEM image of SR-SiNW with rough and tapered surface morphology.