Materials Research Bulletin 74 (2016) 507–510

Contents lists available at ScienceDirect

Materials Research Bulletin

journal homepage: www.elsevier.com/locate/matresbu

Characterization of electronic structures from CdS/Si nanoheterostructure array based on silicon nanoporous pillar array

Yong Li[a,*], Xiao Yan Song[b], Yue Li Song[a], Peng Fei Ji[a], Feng Qun Zhou[a], Ming Li Tian[a], Hong Chun Huang[a], Xin Jian Li[c]

[a] Department of Physics and Solar Energy Research Center, Pingdingshan University, Pingdingshan 467000, PR China
[b] Department of Mathematics and Information Science, North China University of Water Resources and Electric Power, Zhengzhou 450045, PR China
[c] Department of Physics and Laboratory of Material Physics, Zhengzhou University, Zhengzhou 450052, PR China

ARTICLE INFO

Article history:
Received 29 July 2015
Received in revised form 27 October 2015
Accepted 12 November 2015
Available online 17 November 2015

Keywords:
A. Interfaces
B. Chemical synthesis
C. Impedance spectroscopy
D. Electric properties
D. Defects

ABSTRACT

The electronic properties of heterostructures are very important to its applications in the field of optoelectronic devices. Understanding and control of electronic properties are very necessary. CdS/Si nanoheterostructure array have been fabricated through growing CdS nanocrystals on the silicon nanoporous pillar array using a chemical bath deposition method. The electronic properties of CdS nanoheterostructure array have been investigated by the current–voltage, complex impedance spectroscopy and capacitance–voltage techniques. The onset voltages, characteristic frequency and built-in potential are gradually increased with increasing the annealing temperature. It is indicated that the electronic structures of CdS/Si nanoheterostructure array can be tuned through the annealing treatments.

1. Introduction

Heterostructures are still widely investigated because their potential application in the optoelectronic devices, which surface and interface properties play very important role in the electronic properties [1]. As is well known, electronic properties of the electron device are characterized by its main electrical parameters such as barrier height, ideality factor, series resistance, and interface states parameters. The understanding and control of these properties are very crucial to many device applications [2–5]. For example, Huang et al. [6,7] have controlled the injection mode of electrons to tune the electroluminescence through insetting the intermediate layers in the heterostructures.

CdS with the band gap of 2.40 eV at room temperature, is an important II–VI semiconductor compound in the electronic and optoelectronic devices such as solar cells [8,9], light emitting diodes [10] and laser [11]. CdS thin films can be fabricated via several techniques [12–14], such as vacuum evaporation, sputtering, spray pyrolysis, electrodeposition, chemical bath deposition (CBD) method, etc. Among these techniques, CBD method which can be used to produce large area homogeneous films, is a simple, low-cost and safe technique [15]. In the previous works, we have investigated the morphologies, structures and photoluminescence of CdS/Si nanoheterostructure array based on silicon nanoporous pillar array (Si-NPA). As for the photovoltaic properties from CdS/Si nanoheterostructure array, relatively high open circuit voltage has been observed. However, obtained short circuit current is small and obtained energy conversion efficiency is low. In order to investigate the reasons of obtained small short circuit current and low energy conversion efficiency, it is necessary to understand the characterization of electronic structures from CdS/Si nanoheterostructure array.

In the present work, the electronic properties of as-grown and annealed CdS/Si nanoheterostructure array (Si-NPA) at the different temperature have been studied through the current–voltage, complex impedance spectroscopy and capacitance–voltage characteristics. With the increasing annealed temperature, the onset voltages, characteristic frequency and built-in potential are gradually increased and tuned through the annealing treatments.

2. Experiments

The silicon wafers used in this experiment were p-type (111) oriented single crystal silicon wafers (*sc*-Si) with a doping concentration of $\sim 1.0 \times 10^{19}\,cm^{-3}$ and a resistivity of 0.007–0.008 Ω cm, which were cut into 1.0 cm by 1.0 cm pieces and cleaned using the standard RCA methods. Subsequently, the silicon

* Corresponding author.
E-mail address: liyong@pdsu.edu.cn (Y. Li).

http://dx.doi.org/10.1016/j.materresbull.2015.11.023
0025-5408/

wafers were etched through a hydrothermal method. Finally, the piece was taken out and washed thoroughly with de-ionized water. As can be seen, the gray *sc*-Si wafer turned dark black because of the formation of Si-NPA on the surface; the growth details and structural properties of Si-NPA have been described previously [16,17]. CdS thin films were deposited on the Si-NPA using a CBD method. The solution was a mixture of cadmium chloride (0.003 mol), ammonia (15 ml) and de-ionized water (65 ml). The mixture was placed into the bath fixed at 80 °C for 60 min with a magnetic agitation to homogenize the mixture. Next, 5 ml ammonium chloride (0.1 mol/l) and 5 ml thiourea (2 mol/l) were added to the mixture in turn. After 5 min, the Si-NPA was vertically placed into the solution to deposit CdS thin films for 40 min. The samples were taken out and washed thoroughly with de-ionization water and dry in the nitrogen atmosphere. As-grown CdS thin films were homogeneous, yellowish, and with good adherence to the Si-NPA.

To illuminate the effect of annealing temperature on the electronic properties, the annealing treatment were carried out at the range of 200 °C and 500 °C with a step of 100 °C in high-purity argon atmosphere for 60 min. A layer of transparent indium tin oxide (ITO) and a layer of aluminium (Al), respectively, were sputtered on the front side and the back side of CdS/Si nano-heterostructure array to carry out the electrical measurements. The morphological properties of Si-NPA and CdS/Si-NPA was characterized by the field emission scanning electron microscopy (FE-SEM, JSM 6700F) at an acceleration voltage of 15 kV. The current–voltage characteristics were measured with a Keithley SOURCEMETER-2400 in the dark at the room temperature. The impedance measurements and capacitance–voltage were carried out at a RST5200 electrochemical workstation (SRS Instrument Inc., China).

3. Results and discussions

Si-NPA is a silicon hierarchical structure characterized by its regular array of micro-sized, quasi-identical and highly porous silicon pillars, with the pore walls being composed of Si nanocrystals encapsulated by Si dioxide [16]. The morphological properties of the CdS/Si-NPA are shown in Fig. 1. As can be seen from Fig. 1, CdS/Si-NPA maintains the morphologic properties of Si-NPA and reveals that both the pillars and the valleys around the pillars are covered with CdS nanocrystals and a continuous grain membrane of CdS nanocrystals is deposited on Si-NPA. In the previous works, the micro-structural properties of CdS/Si-NPA had been characterized [18,19]. This CdS-Si-NPA nanoheterostructure array with the regular morphology can improve charge separation and transport in the optoelectronic application [20,21] and possesses the low average reflectance of ~10%. So, this CdS/Si nanoheterostructure array might have emerged as one of the most promising candidates in the optoelectronic field. In order to study the electronic properties, ITO layer and Al layer are sputtered on the CdS thin films and silicon, respectively.

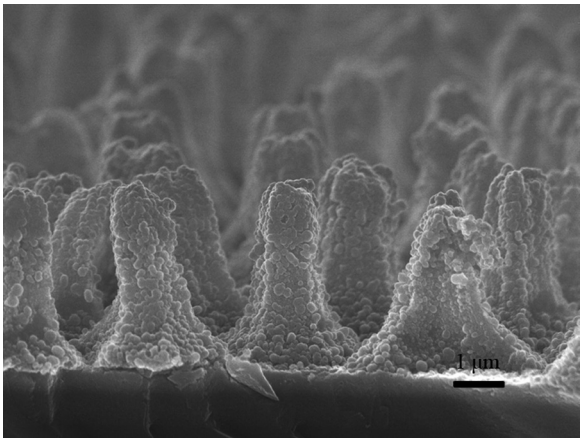

Fig. 1. SEM image of CdS/Si nanoheterostructure array.

The room-temperature dark current–voltage characteristics of as-grown and annealed CdS/Si nanoheterostructure array are shown in Fig. 2. Every current–voltage curve shows obvious rectification effect. The onset voltages are ~1.2 eV, ~1.7 eV, ~1.6 eV,~1.8 eV and ~2.8 eV at a current density of ~1.0mA cm^{-2} for the as-grown and annealed at 200 °C, 300 °C, 400 °C and 500 °C, respectively. Although the onset voltage for annealed sample at 300 °C is slightly reduced, the total variation trend is increased with the increasing annealed temperature. It is indicated that the series resistances of heterojunction are increased with the annealed temperature. The higher annealed temperature results in the much higher defect concentration which will impede the electronic transportation.

The complex impedance spectroscopy is a powerful technique to study and characterize the electrical properties of materials and extract the most important electrical parameters for different materials, which are performed to investigate the electronic transport properties of CdS/Si nanoheterostructure array [22]. Frequency-dependent impedance data are obtained in the range of 1–10^5Hz, and the impedance Cole–Cole plots at room temperature are shown in Fig. 3(a). The shown curves demonstrate only one semicircle, indicating the predominance of a single time constant. And in the complex plane, radius of semicircle is decreasing with the increasing annealing temperature. As can be seen from Fig. 3(a), however, the semicircles are not perfect, which can be ascribed to strong heterogeneity in the device thickness and doping concentration [23].

Fig. 3(b) shows the real part of the complex impedance as a function of frequency at the room temperature. The solid lines indicate the fitting results using the equivalent circuit (inset of Fig. 3(b)), which can be well fitted for all the samples in the whole frequency range. For the as-grown and annealed samples at 200 °C and 300 °C, the real parts of impedance decrease gradually with increasing frequency below ~100 Hz. And above ~100 Hz, the values of real part merge with increasing frequency. However, a plateau region is observed in the annealed samples at 400 °C and 500 °C below ~100 Hz and ~1000 Hz, respectively.

Fig. 3(c) provides the frequency dependent imaginary parts of the impedance spectroscopy. The solid lines in Fig. 3(c) are the fitting results, which can be obtained by the corresponding equivalent circuit (shown in Fig. 3(b)) and shown to be well-fitted over the frequency range. We have observed that the imaginary parts of impedance for the samples show only one peak, suggesting a relaxation mechanism which may originate from the interface of the photovoltaic devices based on CdS/Si nanoheterostructure array [24]. The characteristic frequency $1/\tau_0$ is a frequency where the imaginary part of the impedance is a maximum [23], which can be obtained from Fig. 3(c) for the five samples, namely $1/\tau_0$ are ~5 Hz, ~8 Hz, ~6 Hz, 76 Hz and 759 Hz for the as-grown and annealed at 200 °C, 300 °C, 400 °C and 500 °C, respectively. It is observed that the positions of characteristic frequency peaks are trended to shift to higher frequency as the annealed temperature is increasing. This suggests that the relaxation times are decreased when increasing the annealing temperature.

The capacitance–voltage characteristics of as-grown and annealed CdS/Si nanoheterostructure array at the different temperature in the frequency of 1000 Hz are shown in Fig. 4(a). The properties of capacitance slowly increase with the increasing voltage below ~0.5 V and exponentially increase above ~0.5 V. The variation of capacitances as a function of the voltage implies that