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Viewpoint set

Industrial application of atom probe tomography to semiconductor devices

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ABSTRACT

Advanced semiconductor devices offer a metrology challenge due to their small feature size, diverse composition and intricate structure. Atom probe tomography (APT) is an emerging technique that provides 3D compositional analysis at the atomic-scale; as such, it seems uniquely suited to meet these challenges. However, the semiconductor industry has demanding requirements against which the techniques in use are evaluated. This article explores the use of APT in the semiconductor industry, showing the potential of the technique, the obstacles that occur in practise, and possible future developments.

Introduction

The evolution of the semiconductor industry is shaped by scaling down of critical dimensions and the scaling up of mass production.

To date, semiconductors have reached sizes so small that their lengths can feasibly be counted in numbers of atoms. In addition, recent device geometries have grown in structural complexity and compositional diversity. A modern semiconductor device has an intricate 3D layout and may contain over a fifth of the naturally occurring elements. Analysing the 3D elemental distribution on the near-atomic scale is essential for developing and supervising manufacturing processes for such devices.

Upscaling mass production creates a huge demand for high technology metrology tools. The semiconductor industry is one of the largest worldwide consumers of microscopy equipment, accounting for over a quarter of capital purchases, mostly split between optical microscopes, scanning electron microscopes (SEMs), focused ion beams (FIBs) and transmission electron microscopes (TEMs) [1]. FIBs and TEMs are the cornerstone of advanced semiconductor metrology, typically supported by secondary ion mass-spectrometry (SIMS). Over the past decades, these tools have undergone considerable development to meet the demanding throughputs and cycle times of industry.

Although its origins date back to the 1960s [2], until ten years ago atom probe tomography (APT) had made little impact outside the field of metallurgy. This changed with the availability of commercial tools equipped with lasers, enabling the routine analysis of semiconductors [3,4]. An atom probe combines a field ion microscope with a time-of-flight mass-spectrometer. In order to operate, the material to be studied is fabricated into a needle-shaped specimen with an apex diameter 50–100 nm that will be subjected to a high voltage. This will create an electric field at the apex sufficient that, with the aid of carefully controlled trigger events such as laser pulses, single ions can be field evaporated from the surface and projected towards a position-sensitive detector. From the flight time of the ion, its chemical species can be deduced, while the original position in the specimen can be computed by back-projecting the impact position on the detector. A 3D representation of the component atoms in a small volume can thus be produced. Because of the ability to generate atomic-scale chemical analysis of 3D structures, APT has attracted interest as a technique with the potential to meet the upcoming metrology challenges of the semiconductor industry.

The purpose of this viewpoint article is to discuss the use of APT in the semiconductor industry, and to address the question of whether APT can become an essential industrial tool, or will remain an instrument for niche applications. The article comprises three sections. The first part gives examples from current literature to highlight problems that APT is uniquely suited to solve. The second part surveys the

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challenges that limit success of APT in this role; the third part discusses improvements that can be made in order for APT to reach its potential.

1. Applications/potential of APT to semiconductor devices

The fabrication of a semiconductor device starts with the patterning and deposition of the active silicon regions (*i.e.* channel, source/drain and gate), known as the front-end-of-line (FEOL). This is where the smallest features are found, making them the most challenging to measure. They are the most relevant targets for APT analysis and have dimensions appropriate for the field-of-view (FOV) of the technique. Several examples of elemental distribution analysis by APT on planar-type Si transistor devices [5,6] with high-*k* metal gate stacks [7,8] have been published. In this section, the unique capabilities of APT are highlighted by three exemplary analyses of dopants in actual device geometries.

1.1. Channel dopant fluctuations

As miniaturization progresses, variability originating from the discrete nature of atoms is becoming a challenge for achieving high-yield production. The variability of the threshold voltage (V_T) can be classified into systematic and random components. While the systematic components are caused by process and configuration variability, random dopant fluctuations (RDF) exhibit positional correlation. For certain 65-nm generation metal-oxide semiconductor technologies, V_T random variability in *n*-type devices was found to be larger than in *p*-type ones. While the V_T variability in *p*-type devices can be attributed to RDF, the greater variability in *n*-type devices implies an additional mechanism. APT was used to investigate a planar-type structure from line/space (L/S) patterned wafers (Fig. 1(a)) before and after source/drain extension (SDE) formation [6].

Figs. 1(b) and 1(c) display 3D atom maps of *n*- and *p*-type L/S samples with SDE. The *p*-dopant, B, and *n*-dopants, P and As, can be clearly observed in the gate, SDE, and channel regions. In the *n*-type L/S gate, P atoms segregate at grain boundaries and poly-Si gate/SiO_2 interfaces, while no segregation of B atoms is observed in the *p*-MOS L/S gate. Utilizing the 3D dopant positions enables a statistical analysis of the dopant fluctuations by directly counting the number of atoms. To evaluate the difference in the dopant fluctuations between *n*- and *p*-devices and the impact of SDE formation, the number of dopant atoms in the channel region immediately under the poly-Si gate was counted. Figs. 1(d) and 1(e) show normal probability plots for the number of dopant atoms in a $20 \times 20 \times 30$ nm^3 volume in the respectively doped channel regions. A steeper slope means a smaller dopant fluctuation. In *n*-type samples, the slope has a shallower gradient after SDE formation, indicating that the fluctuation in channel B atoms has increased. In *p*-type samples [Fig. 1(e)], the slope is almost the same before and after, implying that the channel As distribution is not changed by SDE formation.

To clarify the V_T variability in *n*-type devices, the relationship between V_T and channel B concentration was investigated [9]. Starting from devices that underwent electrical characterisation, specimens for APT measurements were fabricated, as shown in Fig. 2(a). In Fig. 2(b), a 3D atom map of a *n*-type device ($V_T = 0.56$ V) is shown. P and As atoms in the gate are segregated at the grain boundaries of the poly-Si and the poly-Si/SiO_2 interface. The channel B concentration to a depth of 30 nm below the gate SiO_2, being the principle active volume for carrier transport when V_T is in the linear regime, shows a positive correlation between V_T and channel B concentration, as shown in Fig. 2(c). However, in addition to the channel dopants, factors like the dopant distribution in other device regions will also contribute to the variation in V_T. A strength of APT is the ability to detect distributions for all elements relevant for doping in order to establish correlations [10].

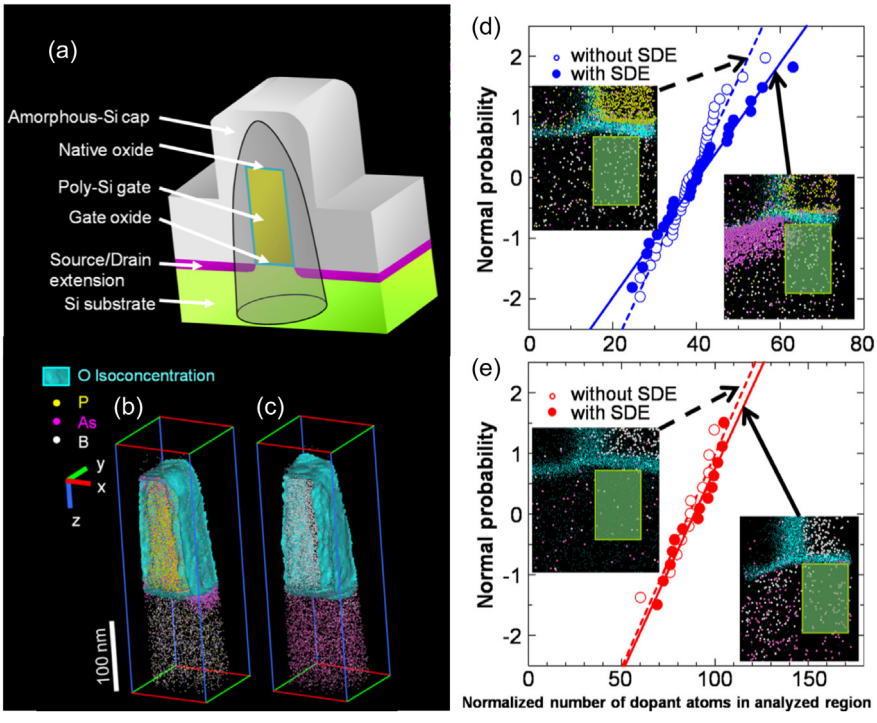

Fig. 1. (a) Schematic illustration of planar device structure (line and space sample) after gate patterning and SDE formation. 3D atom maps of (b) *n*- and (c) *p*-doped devices. Chemical isoconcentration surfaces associated with O highlight the gate surface and gate oxide. P, As, and B, atoms are plotted. Si atoms are not shown for clarity. Normal probability plots of the number of dopant atoms in the channel region of (d) *n*- and (e) *p*-type. Each inset shows projected elemental maps around the extension edge region of *n*- and *p*-types, with and without SDE, (the thickness in the *y* direction is 20 nm). Statistical analysis was performed in the shaded regions just under a gate SiO_2 layer. Solid and broken lines represent the best-fitted plots with and without SDE formation, respectively. The number of dopant atoms is normalized by the atom count in the selected volume.
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