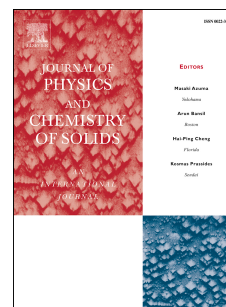


Accepted Manuscript

Cobalt germanide nanostructure formation and memory characteristic enhancement in silicon oxide films

Beom Soo Joo, Hyunseung Kim, Seunghun Jang, Dongwoo Han, Moonsup Han



PII: S0022-3697(18)30120-3

DOI: [10.1016/j.jpcs.2018.04.011](https://doi.org/10.1016/j.jpcs.2018.04.011)

Reference: PCS 8527

To appear in: *Journal of Physics and Chemistry of Solids*

Received Date: 15 January 2018

Revised Date: 14 March 2018

Accepted Date: 12 April 2018

Please cite this article as: B.S. Joo, H. Kim, S. Jang, D. Han, M. Han, Cobalt germanide nanostructure formation and memory characteristic enhancement in silicon oxide films, *Journal of Physics and Chemistry of Solids* (2018), doi: 10.1016/j.jpcs.2018.04.011.

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

Cobalt Germanide Nanostructure Formation and Memory Characteristic Enhancement in Silicon Oxide Films

Beom Soo Joo,¹ Hyunseung Kim,² Seunghun Jang,³ Dongwoo Han,⁴ and Moonsup Han¹

¹*Department of Physics, University of Seoul, Seoul 135-743, Republic of Korea*

²*NAND Tech Development Division, SK Hynix Inc., Icheon 467-701, Republic of Korea*

³*Advanced Materials Division, Korea Research Institute of Chemical Technology, Daejeon 305-343, Republic of Korea*

⁴*The Semiconductor R&D Center, Samsung Electronics Co., Ltd., Gyeonggi-Do 445-701, Republic of Korea*

*Corresponding author's email: mhan@uos.ac.kr

Abstract

We investigated nano-floating gate memory having a charge trap layer (CTL) composed of cobalt germanide nanostructure (ns-CoGe). A tunneling oxide layer; a CTL containing Co, Ge, and Si; and a blocking oxide layer were sequentially deposited on a p-type silicon substrate by RF magnetron sputtering and low-pressure chemical vapor deposition. We optimized the CTL formation conditions by rapid thermal annealing at a somewhat low temperature (about 830°C) by considering the differences in Gibbs free energy and chemical enthalpy among the components. To characterize the charge storage properties, capacitance–voltage (C–V)

Download English Version:

<https://daneshyari.com/en/article/7920201>

Download Persian Version:

<https://daneshyari.com/article/7920201>

[Daneshyari.com](https://daneshyari.com)