Modern Electronic Materials (2016) 2, 23–28

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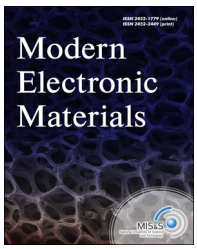

X-ray topographic study of defects in Si-based multilayer epitaxial power devices

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KEYWORDS
X-ray topography;
Silicon;
Defects;
Multilayer epitaxial structures;
Power devices;
Electrical characteristics

Abstract
Silicon based multilayered epitaxial structures are currently the main material for large-scale commercial fabrication of generally used power semiconductor devices such as fast recovery epitaxial diodes (FRED), isolate gate bipolar transistor (IGBT), power MOSFETs etc.
Defects in silicon based multilayer epitaxial structures used as the initial material for power epitaxial-diffusion devices have been studied by X-ray topography techniques. We show that the dislocation nets with nonuniform distribution of dislocations both over thickness and layer square in the form of dense rows (dislocation walls) or slip bands were principal defects in the initial epitaxial layers and have influenced the electrical characteristics of power devices.
The X-ray methods used in the work allow revealing and identifying growth and process defects in device structures, studying their distributions, analyzing their mutual interactions and obtaining valuable information on the nature and evolution of the defects during device structure fabrication processes. This information allowed us to optimize the choice of initial materials and processes aiming to reduce the content of critical electrically active structural defects in the crystals that can influence the parameters of fabricated semiconductor devices; we also increased process yield and tangibly improved semiconductor device operation reliability in severe conditions and emergency modes.

☆This Article was written on the basis of reports presented at XTOP'2012 and Silicon'2012 International Conferences, St. Petersburg.
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Peer review under responsibility of the National University of Science and Technology MISiS.

http://dx.doi.org/10.1016/j.moem.2016.08.004

Introduction

Silicon based multilayered epitaxial structures are currently the main material for large-scale commercial fabrication of generally used power semiconductor devices such as fast recovery epitaxial diodes (FRED), isolate gate bipolar transistor (IGBT), power MOSFETs etc. The annual world market of these device is in excess of $5 bln. Thus, studying the quality of the crystals for revealing defects that impair the electrical properties of the devices and reduce the yield of semiconductor structures is an important practical and economic task. The structural perfection and defects in single crystal silicon and in silicon-based epitaxial and diffusion layers are currently studied using a number of efficient X-ray topography techniques [1,2]. These techniques are nondestructive (by the type of test specimen impact) and allow revealing and identifying growth and process defects in real device structures, studying their distributions, analyzing their mutual interactions and obtaining valuable information on the nature and evolution of the defects during device structure fabrication processes. This information allows one to optimize the choice of initial materials and processes aiming to reduce the content of critical structural electrically active defects in the crystals that can influence the quality and reliability of semiconductor devices.

Due to the relatively low X-ray absorption in the typical wavelength range and the mechanical strength of its single crystals silicon is a good material for X-ray topographic studies. X-ray topography is a powerful tool in the study of real crystalline structure. For X-ray topographic analysis crystals with thick active layers are the most suitable in which the capacities of these techniques can be used to the maximum extent. These structures are for example thick silicon devices in which the active layers are dozens or hundreds microns in thickness and the operation voltages are 7–8 kV or higher. There are however conditions relating to the specific parameters of device structures.

Experimental

We studied the initial multilayered (2–4-layered) epitaxial structures manufactured by Russian companies (EPIEL, SILICON GROUP EL etc.) using gas transport epitaxy at 1070–1200 °C growth temperatures. The epitaxial layers were grown on KES 0.01 and KDB 0.005 Si wafers doped with antimony (KES grade) and boron (KDB grade) to resistivities of 0.008–0.015 and 0.006–0.003 Ω cm, respectively. The wafers were 76 and 100 mm (3 and 4 in.) in diameter and had (100) and (111) orientations. The epitaxial layers were doped during the growth with boron or phosphorus impurities, the electrical resistivity of the layers in the device structures being varied from 0.1 to 100 Ω cm for a single layer thickness of 5–70 μm. Epitaxial layers with different conductivity types were grown in a continuous growth process, the overall thickness of all the epitaxial layers for the fabrication of active *p* and *n* regions of the power devices being varied from 25 to >150 μm for high-voltage device structures. The initial wafer thicknesses for epitaxial growth were 380 and 420 μm for 3 and 4 in. wafers, respectively. Self-doping during epitaxy was suppressed using the well-known epizos and sandwich techniques, the protective layer thicknesses being 15–25 μm. Greater epitaxial layer thicknesses, higher wafer doping and back-side self-doping protection layers for epitaxial growth were the main X-ray topography study implications of our test device structures that predetermined the use of specific techniques.

The main test techniques were the Lang projection technique and the Bragg back reflection technique (similar to the Bragg–Barrett–Newkirk technique) in MoK_α radiation for the transmission setup and in CuK_α radiation for the reflection setup [1,2]. We analyzed a set of reflections from different atomic planes. In addition we used the transmission frame-by-frame technique for heavily asymmetrical reflections when the incident X-ray beam width was 1/3–1/5 of the specimen thickness [3]. This technique provides an estimate of defect distributions in local specimen cross-sections and imaging of the epitaxial layer/substrate boundary.

The back-side protective layers on the test structures produced lattice defects that distorted clear defect images during Lang measurements, so we had to remove these protective layers in some cases. We used free abrasive grinding followed by damaged layer removal by chemical etching or chemical–mechanical polishing. The most probable depth of the epitaxial layer/substrate boundary during structural defect formation was far greater than the thickness of the layer analyzed by X-ray topography. Therefore for back reflection studies of these structures to retrieve defect depth profiles we made angle laps in the specimens. The lap surfaces were at a low angle to epitaxial layer planes. The data collection depth for back reflection studies of dislocation containing specimens was estimated as follows:

$$T = \frac{2{,}3}{\mu[\mathrm{cosec}(\theta+\alpha) + \mathrm{cosec}(\theta-\alpha)]},$$

where μ is the linear photoelectric absorption coefficient for the test X-ray wavelength, θ is the Bragg angle and α is the angle between the reflection plane and the crystal surface. For the most convenient 422 reflection in CuK_α radiation for (100) specimen surface orientation this depth is 18.6 μm. The angle laps were made by grinding the specimens clamped in special holders followed by removal of the grinding damaged layer distorting clear images. In some cases we also removed the top epitaxial layers to obtain misfit dislocation network images near the substrate boundary. Frame-by-frame imaging proved to be very useful for studying final device structures. Despite its moderate resolution this technique provided almost immediate information on whether any dislocations were formed in a specific section of the structure and did not require removing the protective layer. The specimens were examined on domestic URT, DTS and KRS instruments. Topographic patterns were imaged on RT-K photographic film made by Tasma Co., Kazan.

The electrical resistivity and homogeneity of the epitaxial layers were assessed using standard probing techniques for local in-depth and surface doping impurity distribution analysis of epitaxial layers. The measurements were carried out on a VIK-UES SR-16 computing and measurement system made by IKIN Co., Moscow, in the four- and one-probe measurement setups [4,5]. The wafer surface parameters at