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New designs of a complete set of Photonic Crystals logic gates

Hussein M.E. Hussein [a],[*], Tamer A. Ali [a],[b], Nadia H. Rafat [a]

[a] *Department of Engineering Mathematics and Physics, Faculty of Engineering, Cairo University, Giza, Egypt*

[b] *Center for Nanotechnology, Zewail City of Science and Technology, Giza, Egypt*

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ABSTRACT

In this paper, we introduce new designs of all-optical OR, AND, XOR, NOT, NOR, NAND and XNOR logic gates based on the interference effect. The designs are built using 2D square lattice Photonic Crystal (PhC) structure of dielectric rods embedded in air background. The lattice constant, a, and the rod radius, r, are designed to achieve maximum operating range of frequencies using the gap map. We use the Plane Wave Expansion (PWE) method to obtain the band structure and the gap map of the proposed designs. The operating wavelengths achieve a wide band range that varies between 1266.9 nm and 1996 nm with center wavelength at 1550 nm. The Finite-Difference Time-Domain (FDTD) method is used to study the field behavior inside the PhC gates. The gates satisfy their truth tables with reasonable power contrast ratio between logic '1' and logic '0'.

1. Introduction

All-optical integrated circuits are gaining importance in recent years due to their outstanding performance in optical computers, high-speed data processing, and optical networks [1]. Photonic Crystals (PhCs) play a vital role in building optical logic gates in compact sizes to be embedded in optical integrated circuits. Many design techniques for PhC logic gates were reported; such as self-collimated beams [2–6], multi-mode interference [7–11], nonlinear effects [12,13], nematic liquid crystal [14], and interference based gates [15–21].

The self-collimated beams gates need a phase shifter at the inputs of the gate to realize the logic operations, and this requires large footprint [2]. A precise phase control is needed in the multi-mode interference for each input for different logic gates, which is hard to achieve. Although the nonlinear PhC logic gates have the advantages of high contrast ratio between logic '0' and logic '1' [12], their nonlinear properties are triggered by high power consumption with high response time and narrow range of operating frequencies.

In this paper, we introduce new designs of the complete set of the all-optical logic gates based on the interference effect, using 2D square lattice PhC structure. The square lattice exhibits simplicity of design and fabrication. To reduce power consumption, we use linear materials for the PhC structure. The design introduces wide band of operating wavelengths with a center wavelength at $\lambda = 1550$ nm, to be suitable for different applications. We do not use phase shifters, which reduces the footprint of each gate.

2. Design methodology

We propose a design that is based on 2D square lattice PhC structures of germanium (Ge) rods, with a relative permittivity of 16, embedded in a background of air. The contrast ratio between the dielectrics constants of Ge and air is high, which allows wide ranges of operating wavelengths of PhC gates. Ge is also compatible with the conventional CMOS fabrication technology [22].

We use the gap map to select the lattice constant, a, and the rod radius, r [23,24]. We use the Plane Wave Expansion (PWE) method [25–28] to calculate the band structure and the gap maps. The gap maps are plots that show the change of the Photonic Band Gap (PBG) with varying the PhC structure parameters a and r as a ratio of r/a. The gap map shown in Fig. 1 is for the 2D square lattice PhC structure of Ge rods in air background. The light signal is assumed to be of a Transverse Electric (TE) mode. The TE mode is when the light propagates in the 2D surface while the electric field vector oscillates parallel to the rods. The operating wavelength is chosen to be $\lambda = 1550$ nm, which is the most common wavelength in telecommunications at the third telecommunication window [29].

The gap map in Fig. 1 is plotted against the normalized frequency, Ω, on the y-axis. Ω is the operating frequency $\omega/2\pi$ divided by the ratio c/a, where c is the speed of light in space. It is clear from Fig. 1 that the lowest band gap has the widest gap. The maximum gap is realized at $r/a = 0.15$, between $\Omega_1 = 0.4572$ and $\Omega_2 = 0.2902$ with center

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[*] Corresponding author.
E-mail address: hessiun_mohamed@cu.edu.eg (H.M.E. Hussein).

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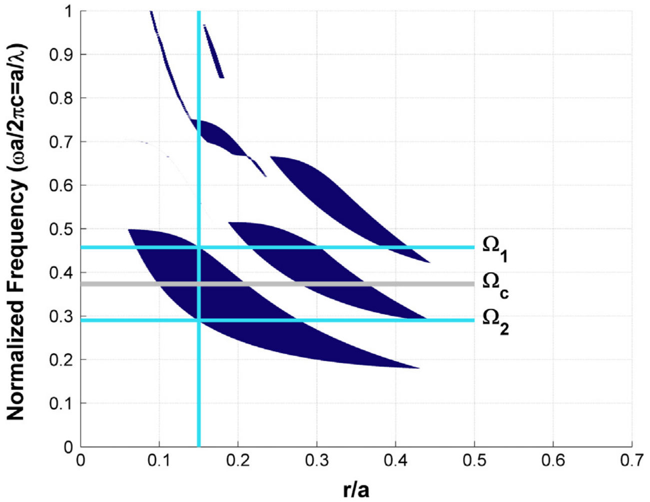

Fig. 1. The gap map of the proposed 2D square lattice PhC logic gate of Ge rods in air background for TE mode.

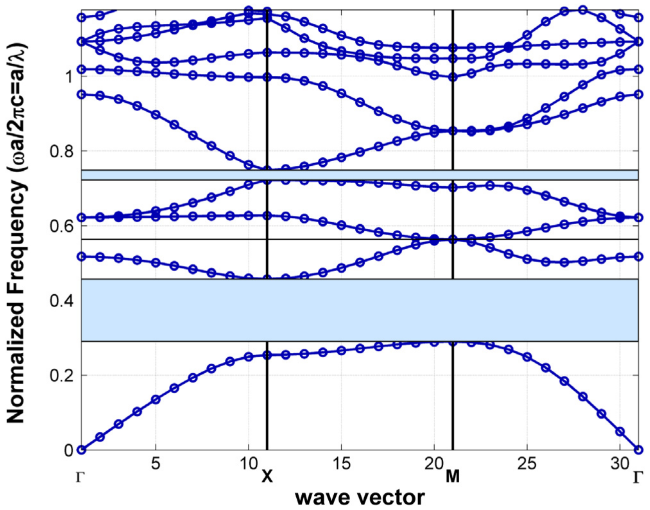

Fig. 2. The band structure of the proposed 2D square lattice PhC logic gate of Ge rods in air background for TE mode at $r/a = 0.15$.

normalized operating frequency $\Omega_c = 0.3737$. Hence, to achieve the center operating wavelength of $\lambda = 1550$ nm, the lattice constant a is designed to be 0.58 μm. The corresponding band structure of the selected design parameters is shown in Fig. 2. According to the selected design parameters, the corresponding range of wavelengths of the band gap is found to be from 1266.9 nm to 1996 nm.

3. Proposed designs and simulation results

The PBGs define the ranges of frequencies that are forbidden to propagate through the PhC structure. Introduced line defects in the PhC structure act as waveguides for signals of the forbidden frequencies. Thus, we can design optical logic gates by tailoring the suitable waveguides for each input to realize the gates functions. Our proposed PhC logic gates are based on the interference effect. In general, logic ‘1’ and logic ‘0’ values are obtained at the output port by introducing constructive and destructive interference, respectively. If the input signals interfere together with a phase difference of $2n\pi$, where n is an integer, this leads to constructive interference. By contrast, if the phase difference of the input signals is $(2n+1)\pi$ where they meet, then a destructive interference occurs. The phase differences in our proposed gates are obtained by creating path differences between the signals.

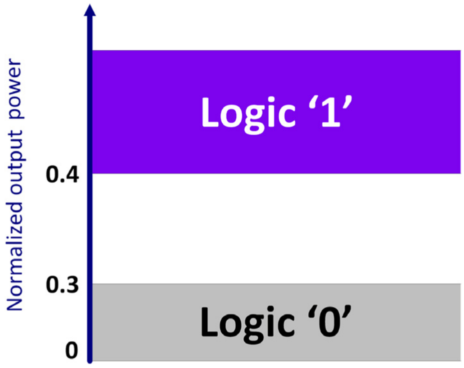

Fig. 3. The range of normalized power values at the output with the corresponding logic.

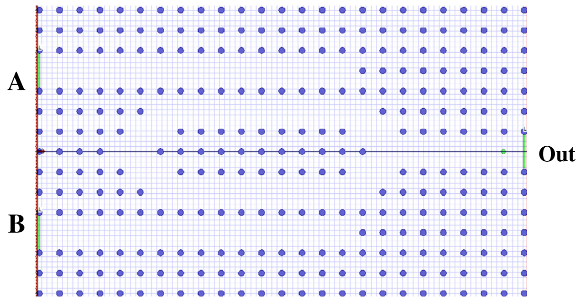

Fig. 4. The proposed 2D OR gate, where A and B are the input ports.

To study the logic gates behavior, we simulate them using the free Finite-Difference Time-Domain simulation software OptiFDTD of Optiwave Systems Inc. [30]. The boundaries of each gate structure is set to Perfectly Matched Layers (PMLs). The gates performance is studied by calculating the Contrast Ratio (CR), which is the ratio between the output powers of logic ‘1’ and logic ‘0’ as follow [10]:

$$CR = 10log(\frac{P_1}{P_0}) \tag{1}$$

where P_1 and P_0 are the power values at the output port for logic ‘1’ and logic ‘0’, respectively. In all of our simulations, we used a light source of power P_o to be launched to the input ports of the gates. The detected power at the output port is considered logic ‘0’ if the power is less than or equal to $0.3P_o$, and is considered logic ‘1’ if the power is greater than or equal to $0.4P_o$, as shown in Fig. 3.

3.1. The OR gate

The proposed OR gate is shown in Fig. 4, where it consists of a resonator with two arms created by removing dielectric rods from the PhC structure to form a defect. Thus, when a wave of an operating frequency inside the PBG is launched into the structure, this wave can be confined and guided. The two arms are the waveguides of the input signals, which are coupled to the resonator via a line of rods. The signal is finally guided through a line defect to the output port. The proposed OR gate possesses an approximate size of 14 μm × 9.44 μm.

Different operations of the OR gate are shown in Fig. 5, and the truth table together with the output power are shown in Table 1. When an input signal only at input A is launched, the wave will be guided in the upper waveguide till it couples with the resonator. When the coupling occur, a part of the signal propagates inside the resonator in the ClockWise (CW) direction while the other part propagates in the Counter ClockWise (CCW) direction, where these two parts eventually