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Bias current influence on semiconductor optical amplifier's equivalent circuit

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ABSTRACT

The equivalent electrical circuits – including the parasitic elements and their variations with the injected bias current – for three semiconductor optical amplifiers (SOA) were obtained. Frequency domain measurements with further tuning of numerical modeling parameters were used to extract circuit parameters. Characterization of chip-on-carrier and encapsulated devices agree with numerical data up to 20 GHz. The results are relevant for designing fast speed, SOA-gated switches in optical routers.

1. Introduction

Semiconductor optical amplifiers (SOAs) have been used in the last few years with several functionalities besides amplification. SOAs are being considered as all-optical wavelength converters with regeneration capabilities [1,2], also for optical carrier wavelength reuse in high bit rates passive optical networks [3,4], optical packet networks [5], high speed optical routers [6] and in electro-optical switches [7,8]. The SOA steady-state and dynamic operations can be investigated by analytical and numerical models [9–13], including equivalent electrical circuit analysis [14]. This last approach may include gain compression effects and parasitic capacitances/inductances descriptions, and be solved by circuit analysis tools. The SOA is essentially a semiconductor laser with anti-reflective coatings on its edges [15], so previous models for diode lasers [16–19] were used as basis to obtain the SOA equivalent circuit, including operation below and above the transparency condition.

Previous works relied on similar models to achieve the equivalent electrical circuit for a chip-on-carrier (COC) SOA [20]. Here the investigation of the SOA's high frequency impedance behavior including its parasitic elements (added by mounting and coupling) is accomplished including its variation with the DC bias currents (I_{bias}). Also the circuit parameters characterization up to 20 GHz are presented for a COC-SOA and for two hermetically encapsulated SOAs, Supplementary analysis shows the influence of the SOA's active cavity length and carrier lifetime.

2. Experimental procedure

The SOA electrical impedance measurements covered spectra from few kHz up to 20 GHz. The experimental setup is basically composed by the SOA under test mounted in a microwave matching feeder. The setup is connected to a 40 GHz Network Analyzer including a bias-t and an electrical bias current source. The SOA injection current (I_{bias}) was varied from 0 to 110 mA, and the current–voltage (I–V) characteristics of devices were also obtained. Two encapsulated SOA were tested: the *Pack-SOA.1*, a 2 mm long cavity device (*CIP, NL-OEC-1550*, maximum drive current of 400 mA, saturation output power of 6 dB m, maximum gain of 34 dB) and the *Pack-SOA.2* with cavity length of 650 μm (*InPhenix, IPSAD1503*, maximum drive current of 350 mA, saturation output power of 5 dB m, maximum gain of 16 dB). Operating temperature of the packaged SOAs is controlled through the built-in thermistors and thermoelectric coolers. The output power as a function of bias current for the SOAs used in this work are illustrated in Fig. 1; the laser output power is fixed at −5 dB m for packaged SOAs and +10 dB m for COC-SOA. All SOAs are InP

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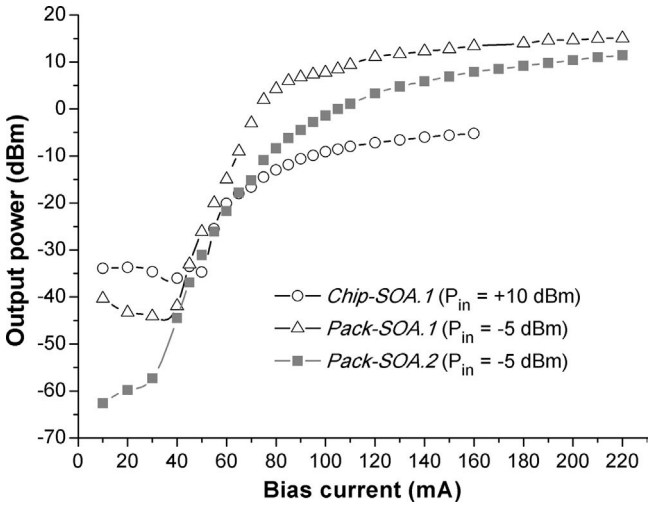

Fig. 1. SOAs' output power versus bias current for constant input power.

buried heterostructure design. The tested COC-SOA, called *Chip-SOA.1* has the same SOA chip as *Pack-SOA.1*.

The encapsulated and COC SOAs microwave connections (not to scale) are shown at Figs. 2 and 3, respectively. The encapsulated SOAs microwave connections inside the butterfly package are shown schematically (not to scale) in Fig. 2. Both butterfly pins enters the enclosure and are connected to the SOA using gold wires in a series of 5 steps. Those steps of wires and metallic plates increase the parasitic inductances and capacitances when comparing with the COC-SOA mount (Fig. 3). To provide a precise temperature control a Peltier element is attached close to the SOA chip, also increasing parasitic. The microwave connection (not shown here) is provided by a 50 mm length of 0.085 in. diameter PTFE semi-rigid coaxial cable in series with a 47 Ω, low inductance resistor and a 5 mm length strip line soldered to the butterfly outside pin (shortened to 2 mm). Therefore, both the butterfly internal connections and the external connections contribute to a higher parasitic for the encapsulated devices. We used 3.5 mm microwave connectors.

The COC mounting of Fig. 3 uses a microstrip line (16 mm length with alumina substrate) connected in series to a low inductance 47 Ω resistor. The other resistor terminal is attached directly to a SOA chip-on-carrier constructed on silicon ($10 \times 2 \times 1$ mm^3). The SOA electrical terminals are connected on both sides of the carrier by gold wires over gold plates, the ground plane is bounded directly over one of these plates. The Peltier element is a 10 W device able to control temperature for the whole microwave metallic enclosure ($40 \times 15 \times 20$ mm^3). The input (output) light is coupled into (from) the COC-SOA using fiber lenses positioned by 5-axis piezo actuators, all stabilized in an optical table [21], with total coupling loss of 15 dB. The bias-t is constructed inside the microwave enclosure.

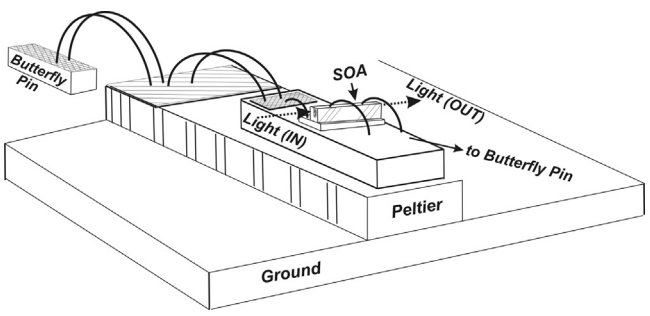

Fig. 2. Schematic of packaged SOAs connections (not to scale).

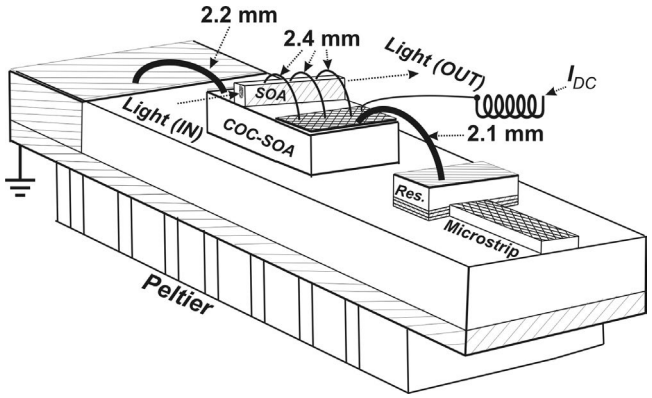

Fig. 3. *Chip-SOA.1* in series with a low inductance resistor (47 Ω) and a microstrip line (not to scale).

A movable low inductance gold contact was used to short-circuit the SOA electrical inputs. In Fig. 3, the movable contact goes from the metallic plate (were the 2.4 mm wires are soldered) up to the earth metallic plate (were the 2.2 mm wire is soldered). This can isolate the SOA from the RF feed line and the series resistor during the impedance measurements, enabling to obtain the parameters of the microwave mounting without the SOA. However, the SOA chip was not directly available to be short-circuited. Therefore the 2.4 mm wires, the 2.2 mm wire, and the SOA chip-on-carrier parasitic elements should be included in the SOA chip equivalent circuit obtained here, and we call this COC parasitics. The experimental values were transferred to the equivalent circuit software analyses (*Agilent* ADS) [22], allowing the comparison between theoretical (simulated) and experimental results, up to 20 GHz. Beyond this frequency, the simulated/experimental phase impedance agreement was difficult to set, and it is not shown here. However the 20 GHz bandwidth is adequate for the study of practical SOA electro-optical switching times around hundreds of ps [8].

3. Equivalent circuit modeling

The equivalent electrical circuit used here was based on semiconductor lasers modeling. The structural locations of parasitic elements are illustrated in Fig. 4 for an etched mesa buried heterostructure (EMBH) laser [16–19]. Given the similarities with the tested SOAs, we adopted the parameters for an EMBH device.

The resistances in series with the active region ($R_{SP}+R_{SS}$) are the dominant parasitic elements, and also there are three main capacitive leakage paths at high frequencies [18]: the MIS capacitance (C_N) distributed across the entire chip; the reverse-biased

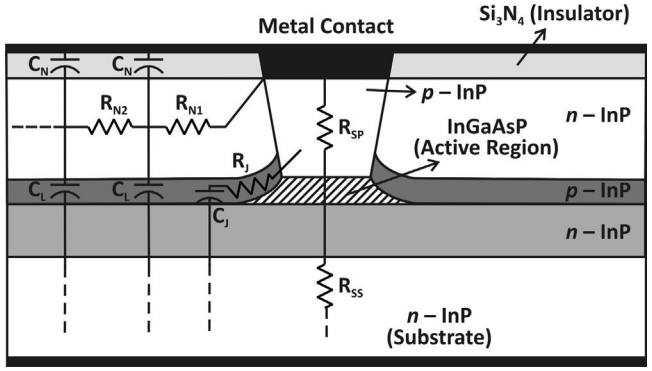

Fig. 4. Cross-sectional view of an EMBH laser with parasitic elements included (adapted from [16,17]).