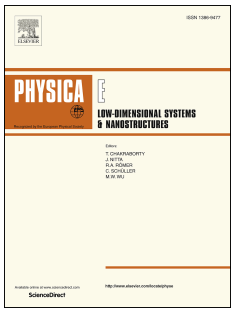
Accepted Manuscript



Semi-analytical modeling of high performance nano-scale complementary logic gates utilizing ballistic carbon nanotube transistors

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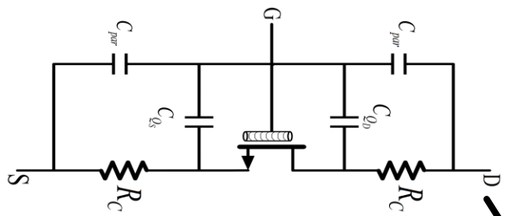
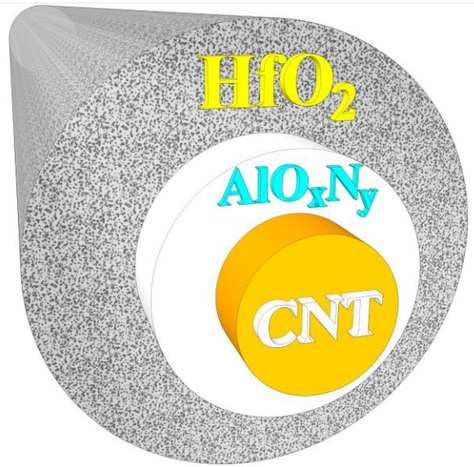
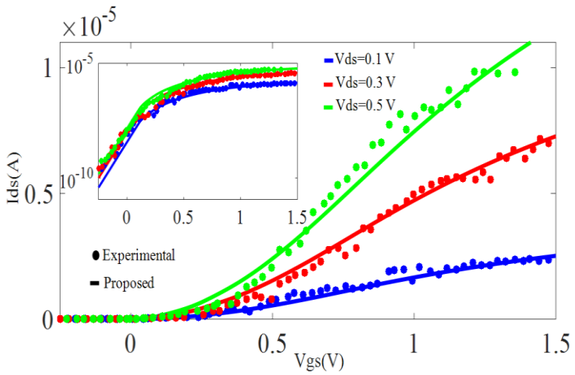
Semi-analytical
Device Modeling





Gate-all-Around
CNFET



I-V Characteristics

Basic Logic
Gates

Proposed Model
Benchmarking

Half Adder