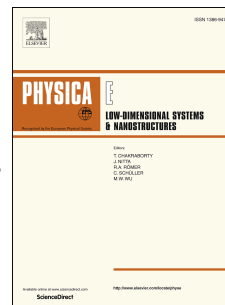


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Semi-analytical modeling of high performance nano-scale complementary logic gates utilizing ballistic carbon nanotube transistors

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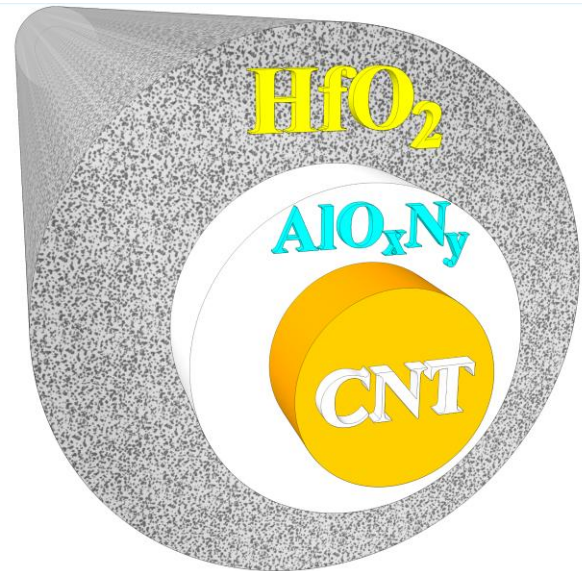
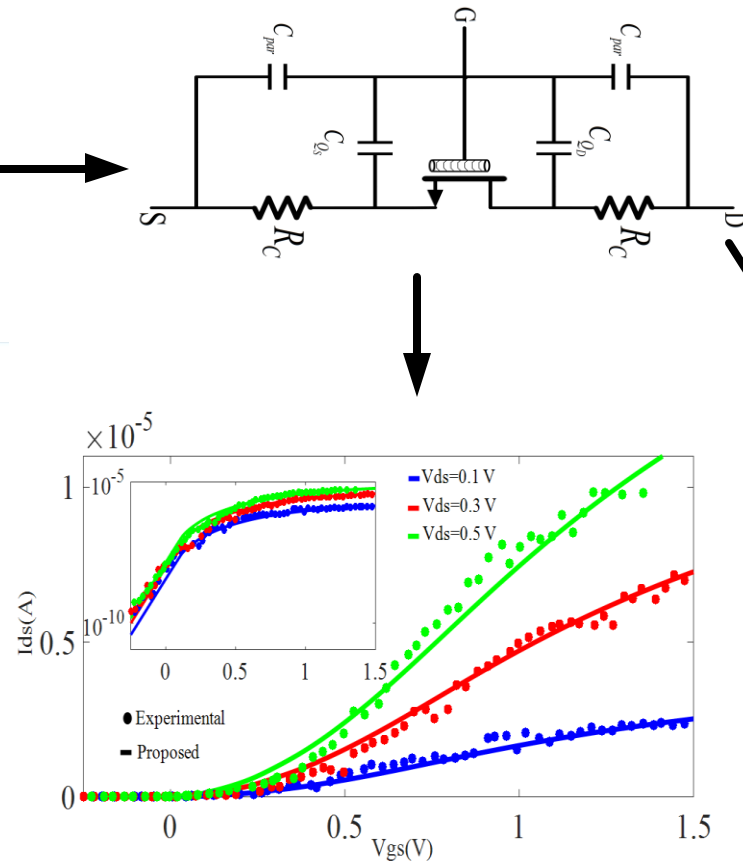
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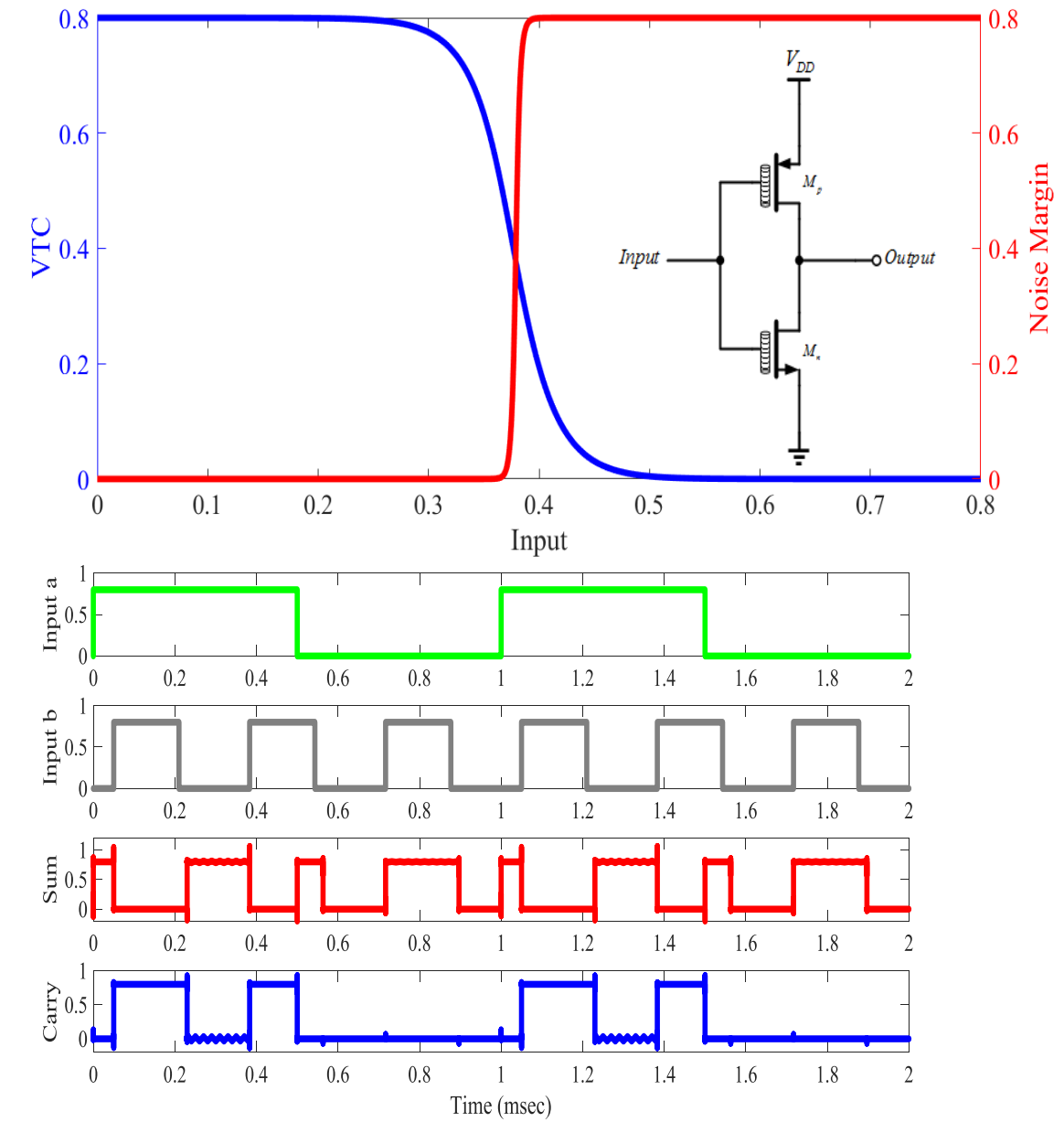
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Semi-analytical
Device ModelingGate-all-Around
CNFET

I-V Characteristics

Basic Logic
GatesProposed Model
Benchmarking

Half Adder



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