Solar Energy Materials & Solar Cells 94 (2010) 1506–1511

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Excellent antireflection properties of vertical silicon nanowire arrays

Sanjay K. Srivastava [a,*], Dinesh Kumar [a], P.K. Singh [a], M. Kar [a], Vikram Kumar [a], M. Husain [b]

[a] National Physical Laboratory, Dr. K.S. Krishnan Marg, New Delhi-110012, India
[b] Department of Physics, Faculty of Natural Sciences, Jamia Millia Islamia, New Delhi-110025, India

ARTICLE INFO

Article history:
Received 29 June 2009
Received in revised form
29 December 2009
Accepted 21 February 2010
Available online 20 March 2010

Keywords:
Silicon nanowires
Metal induced etching
Black silicon
Antireflective coatings (ARC)

ABSTRACT

We report a simple approach to prepare cost effective antireflective surface directly on silicon wafers, which consists of arrays of vertically aligned silicon nanowires (VA-SiNWA). Large area VA-SiNWA were realized by silver induced wet chemical etching of p-silicon (1 0 0) substrates in aqueous HF and $AgNO_3$ solution at room temperature. Length of Si wires (diameter in 50–300 nm range) was found to increase linearly with etching time (0–120 min). A remarkable reduction in reflectivity (R_λ) for surfaces with Si wires was observed. The value of R_λ less than 2% was realized in the 300–600 nm wavelength range in the case of ~12 μm long Si wires, a value better than the best R_λ reported in anisotropically textured surface or single layer antireflection coatings. The VA-SiNWA behaves as a subwavelength structured surface that could suppress the reflectivity to a great extent. Such surfaces may have potential applications as antireflection surface for silicon solar cells.

1. Introduction

Surface antireflection techniques are important for improving the performance of many optical and optoelectronic devices such as solar cells, planar displays, videos, camera monitors, and light sensors [1–3]. For example, flat silicon surfaces have high reflectivity (35–40%) with a strong spectral dependence, which limits the power conversion efficiency of silicon based solar cells. Usually, transparent quarter wavelength layers of SiO_x, TiO_x, or Si_xN_y with intermediate or gradient refractive indices are used as antireflection coatings (ARC) [4]. ARC is formed by single or multiple layer film deposition through various processes such as plasma enhanced chemical vapor deposition, sputtering processes, wet coating, sol-gel methods, etc.. These coatings have resonant structures and work effectively only in a limited spectral range and for specific angles of incidence [4]. Also, these coatings have several problems such as thermal mismatch, adhesiveness, stability, etc. In the case of silicon solar cells, a variety of other approaches have also been developed to minimize the reflection losses through modifying surface morphology [3–6] wherein reflection losses in a broad spectral range are reduced by surface texturing by anisotropic etching generally in aqueous alkaline solution. However, this process is limited to single crystalline silicon only [4,7]. An alternate approach to minimize reflectivity (R_λ) utilizes a fine surface textured surface, comprising features on the nanometer scale. Porous silicon (PS) is one such approach to reduce R_λ in the range of 5–8% [8,9]. However, reproduction and fragile nature of the PS layer have always been a matter of concern [6].

Recently, antireflection surfaces based on subwavelength structures (SWSs) have also been investigated [10]. The SWSs are the surface relief structures with dimensions smaller than the wavelength of the incident light. An SWS surface with a deep and tapered profile can suppress the Fresnel reflection substantially over a wide spectral bandwidth. These layers are intrinsically more stable than multilayer ARCs since no layers of foreign materials are involved. It has been shown that optical thickness of the SWS layer to wavelength ratio greater than 0.4 drastically reduces reflection losses and the R_λ approaches zero though it fluctuates slightly at times on further increase of the SWS height [11,12]. For ideal SWSs with near zero reflectivity requires perfectly tapered V-shaped grooves of the SWSs [13].

To date, different methods have been employed to fabricate SWS surfaces [10–15]. Dry etching methods such as reactive ion etching, nanoimprint lithography, etc. are commonly used for the fabrication of SWSs, in which imprinting or shadow masks with resolutions in subwavelength scale are required [10,12,13,16,17]. The masks can be obtained by electron beam lithography (EBL) [10], by laser interference lithography [12, 16], self-assembly like alumina template [13] or from nature materials [17]. However, the low throughput and the cost, for example of the EBL, are of great concerns [10,18]. On the other hand, interference lithography [19,20] and nanoimprint lithography [16] enable the creation of antireflective SWS over large areas but are complex and expensive, hence limiting their applications.

In this paper, we propose a simple, low cost process to produce antireflective surface consisting of vertically aligned silicon nanowires arrays (VA-SiNWA), which clearly resembles SWSs

* Corresponding author. Tel.: +91 11 45608617; fax: +91 11 45609310.
E-mail address: srivassk@mail.nplindia.ernet.in (S.K. Srivastava).

0927-0248/$ - see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.solmat.2010.02.033

surface. The Si wires are fabricated at room temperature through metal-induced selective etching of silicon wafers in aqueous HF solution [21]. The growth and morphology of VA-SiNWA and the corresponding reflectivity of the silicon surface with etching time have been investigated and are correlated with the surface morphology.

2. Experiment

Growth of VA-SiNWA was carried out on (1 0 0) p-type (1–5 Ω cm), chemically–mechanically polished (CMP), B-doped crystalline silicon wafers. The etching of 300 ± 10 μm thick wafers was carried out in a teflon vessel containing 5 mol L^{-1} aqueous HF solution and 0.02 mol L^{-1} $AgNO_3$ at room temperature for different etching times. Prior to etching, silicon wafers were sequentially cleaned with acetone, de-ionized water, and boiled in piranha solution (H_2SO_4: H_2O_2=3:1 by volume for 30 min) followed by rinsing with de-ionized water and 5% HF dip to remove oxide. The cleaned silicon wafers were etched for different time durations keeping all other parameters such as concentration of the solution, volume, temperature, etc. constant. The samples surfaces obtained after etching were found to be wrapped with a thick silver (Ag) layer, which consisted of high density tree-like dendritic structures. To remove the Ag layer completely, the as-prepared samples were treated in a conventional Ag etchant solution consisting of NH_3OH: H_2O_2 in the ratio of 3:1 by volume and were rinsed with de-ionized water. After being blown dry in air they were subjected to further investigations. Morphology of the samples was examined by scanning electron microscope (SEM) (LEO model 440VP) and the reflectivity measurements were carried out by spectrophotometer (Shimadzu-UV model 3101PC) in the 300–1100 nm wavelength range.

3. Results and discussion

Typical SEM images of etched silicon wafer are shown in Fig. 1. The low magnification top view of the silicon surface etched for 45 min is shown in Fig. 1a and the corresponding cross-sectional view in the inset. The highly magnified and tilted view of the sample is shown in Fig. 1b. The SEM images indicate that etched silicon wafers consist of dense and vertically aligned one-dimensional nanostructures (VA-SiNWA). From the top tilted view of SEM image shown, surface relief structures with dimensions less than the wavelength of visible light could be seen. The diameters of the Si wires are estimated to be in the range of 50–300 nm by SEM investigations. With increasing etching time, length of the nanowires increased from few nanometers to several micrometers depending on the etching time. The dimensions of the nanostructures, particularly the diameter, remain almost the same throughout the length as can be seen from Fig. 2a and b for etching times of 5 and 45 min where the nanowires length are ~1 and ~12 μm, respectively. It has been found that the length (as determined from cross-sectional view of SEM images) of Si wires increases linearly with etching time for durations (0–120 min), and arrays length vs. etching time curve is shown in Fig. 2c. The estimated average etching rate is ~250 nm min^{-1} for HF and $AgNO_3$ concentration of 5 and 0.02 mol L^{-1}, respectively, at 300 K. The plot clearly indicates that VA-SiNWA of tunable length can be fabricated at room temperature by controlling the etching time.

Fig. 3a–d shows the SEM images (top and tilted view) of VA-SiNWA surfaces fabricated for 2, 5, 15, and 45 min where regions with bright contrast correspond to un-etched silicon surface and with black contrast to the etched regions of the

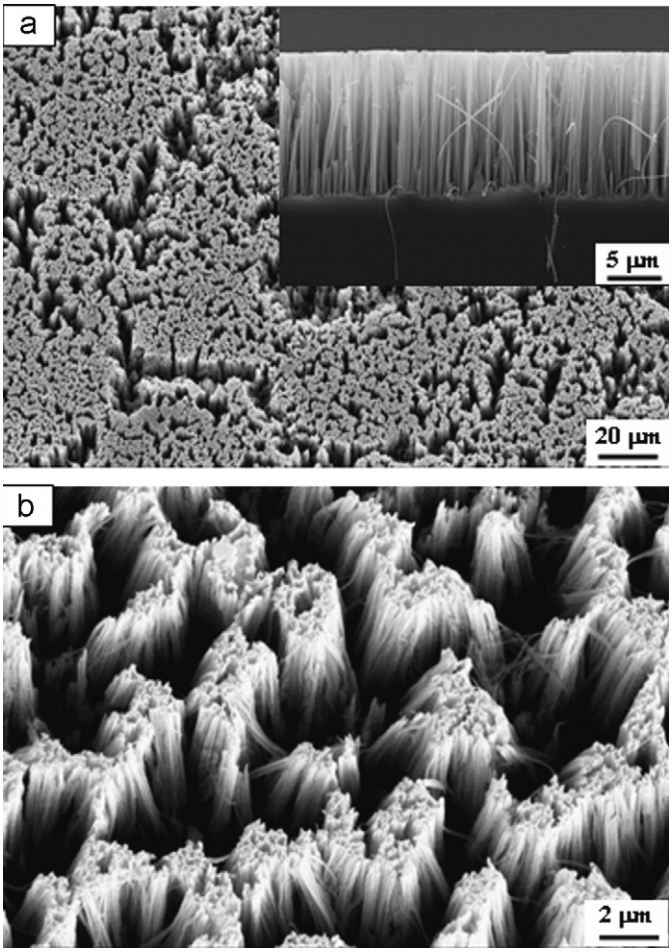

Fig. 1. SEM images of VA-SiNWA obtained after 45 min etching showing (a) top view and the inset shows the cross-sectional view of Si wires of length ~12 μm, and (b) magnified tilted view with angle of tilt 12°.

samples. Fig. 3a shows uniformly distributed nanostructures of low dimensions across the whole area at the onset of etching process. With increase in etching time, etched regions seem to sink deeper and deeper, resulting in the evolution of un-etched silicon regions as one-dimensional structure with diameter in nanometer scale. As the etching progresses, etching of nanowires may also take place due to etching from the top surfaces of the wires that result in the increase of porosity, particularly in the region that are exposed to the etching solutions for longer durations (i.e. close to the top surface). It is noted that with increase in wire length, porosity is more at the top compared to its value at the bottom (Fig. 3d). The porosity was estimated by the image processing method (i.e. top un-etched surface area) of SEM images. The porosity vs. etching time is shown in the inset of Fig. 3b, which shows sharp increase in porosity initially and tend to slow down for larger etching times. The top region porosity was estimated to be ~32% in the sample etched for 2 min whereas its value increased to ~65% for the sample etched for 45 min. It is important to point out that porosity at the Si nanowires–Si substrate interface should remain almost the same (~32%) in all the samples etched for different time durations. It is expected since the density of silicon nanowires attached to the silicon surface remains almost the same with increase in etching duration as is evident from the cross-sectional view of the nanowires shown in Fig. 2a and b. In addition, it is evident that after a certain length, the nanowires could not support themselves to stand vertically of their own and lean over surrounding wires for