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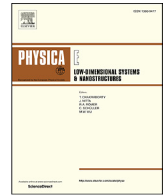

Fast and slow traps in Al_2O_3/(GaN)/AlGaN/GaN heterostructures studied by conductance technique

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ABSTRACT

Influence of interface traps at Al_2O_3/(GaN)/AlGaN interface at low and high frequency on equivalent parallel conductance of Al_2O_3/(GaN)/AlGaN/GaN heterostructure capacitor was studied. By the conductance measurements two types of traps were identified in the measured structure. The traps differ in time constants by more than one order in magnitude. Fast traps with low time constants have narrow energy distribution and are probably located in the semiconductor energy gap close to the insulator semiconductor interface. Slow traps have wider distribution and are assumed to be directly at the insulator semiconductor interface. The presence of the fast traps which are able to respond to external ac signal is given into connection with the recently published increase of the structure capacitance in the plateau region with decreasing frequency.

1. Introduction

GaN based III-N heterostructures are an object of intensive study during recent years, since these materials are applicable for high frequency, high power and high temperature devices. Heterojunction transistors usually use Schottky gate diode. Since the transistors with the Schottky gate have some disadvantages as large leakage currents, current instability, etc., structures with thin dielectric films under the metal gate MISHFET (Metal Insulator Semiconductor Field Effect Transistor) are also studied [1–3]. Such structures have one new interface – between the dielectric and the semiconductor at which electron states in the semiconductor gap occur. These localized states are occupied according to the Fermi level position at the interface and modify the potential distribution in the semiconductor. These states may have a discrete character in energy or which is more probable have a continuous distribution in the semiconductor energy gap. Their presence changes external voltage needed to empty two-dimensional electron gas (2DEG) and in this way their modify threshold voltage of transistors. There may be also fluctuations in interfacial and/or insulator charge that would suggest interfacial charge nonuniformities [4]. They are most often studied by capacitance – voltage (*C-V*) measurement. Ability of interface traps to exchange the charge with the semiconductor depends on the frequency of the measuring signal [5].

Another method for studying the presence of interface traps and their properties is conductance measurement [6,7]. The charge exchange between the interface traps and the semiconductor is connected not only with the capacitance but also with loses which are represented by a resistance in series with the capacitance of the traps. Interpretation of the conductance measurement is more straightforward than the capacitance measurement since there is no necessity to know the capacitance of the semiconductor without interface traps. The impedance of the structure is obviously measured as a parallel combination of the measured capacitance C_m and conductance G_m.

In this paper, we analyze frequency dependent equivalent parallel conduction measurement of the structures and we show that the traps present in the structure may be divided into "fast traps" and "slow traps." The fast traps may be also responsible for the capacitance increase with decreasing frequency [8].

2. Experimental

The structures for measurement were prepared on Si substrates. AlGaN barrier has composition with 25% of Al and was 20 nm thick. On the top there was 2 nm thick GaN cap layer. Dielectric layer Al_2O_3 was deposited by atomic layer deposition (ALD) at 100 °C and its thickness was 20 nm. Then the HEMT devices were formed on the top and the capacitance was measured between gate (G) and drain (D) electrodes. The gate area was 5.65×10^{-4} cm^{-2}. The topology of the structure is shown in (Fig. 1). The capacitors were formed by UV photolithography, electron beam evaporation and lift-off technique.

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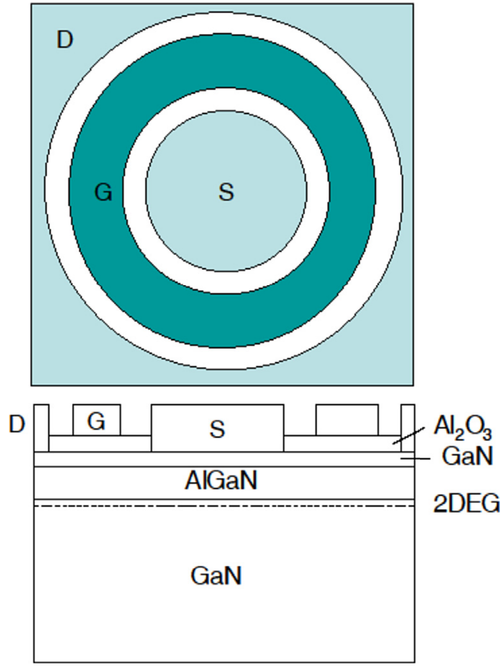

Fig. 1. Topology of the measured structure.

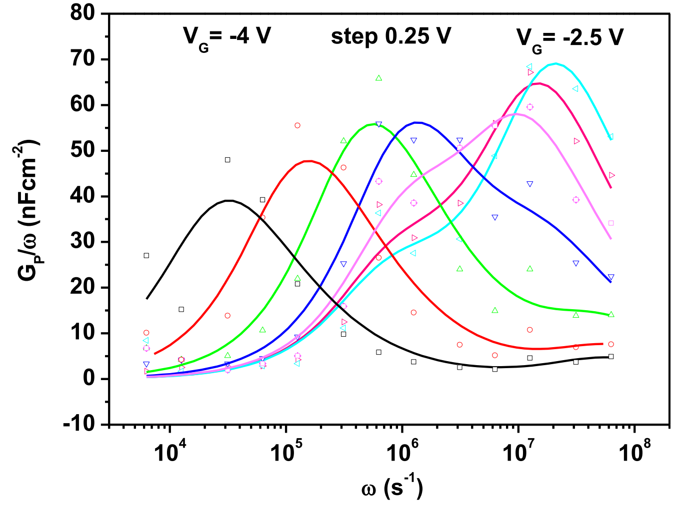

Fig. 2. Equivalent parallel conductance of the structure for different depletion biases.

3. Results and discussion

We have measured and analyzed frequency dependent conductance (*G-V*) curves. Calculation of the equivalent parallel conductance with elimination of the oxide capacitance C_{ox} from the measured C_m and G_m was made according to [9]

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{1}$$

where G_P is the equivalent parallel conductance, G_m is the measured conductance, C_{ox} is the oxide capacitance and C_m is the measured capacitance. The plots of calculated G_P/ω- ω for frequencies ranging from 1 kHz to 5 MHz and depletion voltages from −2.4 to −4 V are in Fig. 2. It is seen that the curves cannot be well enough approximated by a single peaked curve

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right]. \tag{2}$$

For reverse bias around −3 V assuming a continuous distribution of interface traps at the interface, where D_{it} is interface trap density and τ_{it} is the interface trap time constant. The G_P/ω- ω curve has visibly two peaks and that is why we used corrected model which assumed two different distributions of traps [10,11]

$$\frac{G_P}{\omega} = \frac{qD_{it1}}{2\omega\tau_{it1}} \ln\left[1 + (\omega\tau_{it1})^2\right] + \frac{qD_{it2}}{2\omega\tau_{it2}} \ln\left[1 + (\omega\tau_{it2})^2\right]. \tag{3}$$

In Fig. 3 the two peaks for two different bias voltages are analyzed. It is seen that moving the Fermi energy closer to the conduction band the traps with lower τ_{it} become higher in density than the traps with larger τ_{it}. The extracted values of D_{it} and τ_{it} are in Table 1. According to the calculated time constants, the interface traps may be divided into “slow states” with the constant ~10^{-6} s and “fast states” with the time constant ~10^{-7} s. The trap energy level related to the conduction band minimum can be determined from the Schockley-Read-Hall statistics [9,12]

$$E_T = kT \ln(\sigma_T N_C v_t \tau_T), \tag{4}$$

where σ_T is the capture cross-section of the trap, N_C is the density of states

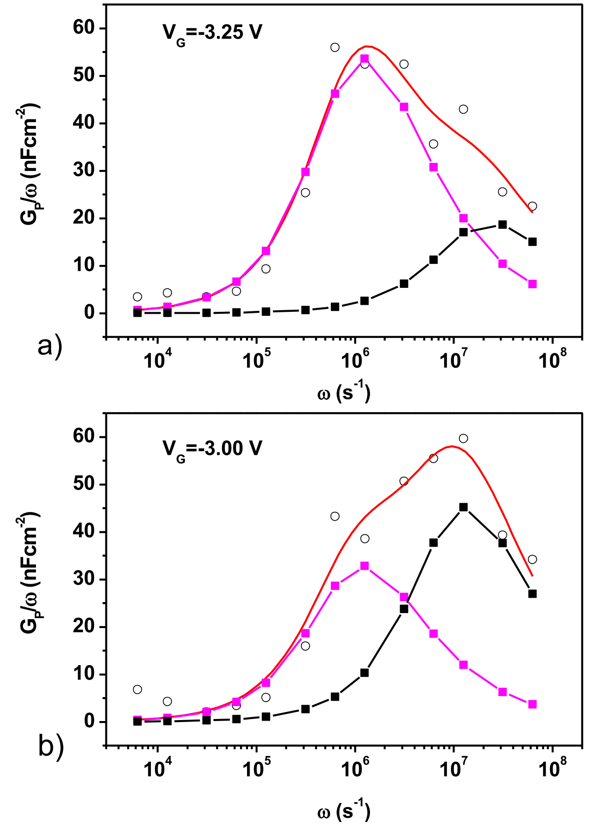

Fig. 3. Change of the peaks of equivalent parallel conductance with external bias.

in the conduction band, ν_t is the carrier thermal velocity. For T = 300 K, $\nu_t = 2.6 \times 10^7$ cm s^{-1}, $N_C = 2.7 \times 10^{18}$ cm^{-3} and $\sigma_T = 1 \times 10^{-14}$ cm^2 [13].

In Fig. 4 the calculated trap density D_{it} in part of the energy gap is shown. The fast traps are located within a narrow energy interval 0.26 and 0.29 eV below the conduction band minimum (CBM). The fact that by changing the external voltage and therefore moving the Fermi level in the semiconductor the energy of the trap does not change significantly implicates that the trap is distributed in the volume and at different applied voltage the trap from the different depth responses to the signal. These traps may be located in the AlGaN barrier layer or in the insulator as so called “border traps” near the semiconductor insulator interface.

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