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Original Research

# Dielectric properties, electrical modulus and current transport mechanisms of Au/ZnO/n-Si structures

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ABSTRACT

Au/ZnO/n-Si (MIS) structures were fabricated by using the RF sputtering method and their complex dielectric constant ($\varepsilon^* = \varepsilon' - j\varepsilon''$), electric modulus ($M^* = M' + jM''$) and electrical conductivity ($\sigma = \sigma_{dc} + \sigma_{ac}$) values were investigated as a function of frequency (0.7 kHz-1 MHz) and voltage (−6 – (+6 V)) by capacitance-voltage (*C-V*) and conductance-voltage (G/ω-V) measurements to get more information on the conduction mechanisms and formation of barrier height between Au and n-Si. The ln$\sigma$-Ln$f$ plots have two different regions corresponding to low-intermediate and high frequencies. Such behavior of ln$\sigma$−ln$f$ plots shows that the existence of two different conduction mechanisms (CMs) at low-intermediate and high frequencies. Moreover, the reverse bias saturation current ($I_o$), ideality factor ($n$), barrier height ($\Phi_{Bo}$) were determined from the forward bias *I-V* data and they were found as a strong function of temperature. The value of $n$ especially at low temperature is considerably higher than unity. The values of $\overline{\Phi}_{BO}$ and standard deviation($\sigma_s$) were found from the intercept and slope of $\Phi_{Bo}$ -$q/2kT$ plots as 0.551 eV and 0.075 V for the region I (80–220 K) and 1.126 eV and 0.053 V for the region II (220–400 K), respectively. The values of $\overline{\Phi}_{Bo}$ and effective Richardson constant ($A^*$) were found from slope and intercept of activation energy plots as 0.564 eV and 101.084 $Acm^{-2}\,K^{-2}$ for the region I and 1.136 eV and 41.87 $Acm^{-2}\,K^{-2}$ for the region II, respectively. These results confirm that the current-voltage-temperature (*I-V-T*) characteristics of the fabricated Au/ZnO/n-Si SBDs can satisfactorily be explained on the basis of TE theory with double GD of the BHs.

## 1. Introduction

MS structures with insulator or oxide layer (MIS/MOS) are produced by sandwiching an interfacial layer such as $SiO_2$, $Si_3N_4$, $SnO_2$, $HfO_2$, $TiO_2$, $Bi_4Ti_3O_{12}$ (BTO), GO-doped PrBaCoO between metal and semiconductor [1–3]. Owing to the technical importance of these devices, the investigation of their electronic properties attracts great interest as a research topic. The electronic properties of MIS/MOS structure depend upon the conditions of surface preparation and forming of these interfacial layers [4–7]. Usually the quality of these structures can be affected by such parameters as surface states or traps ($N_{ss}$) located at interfacial layer, series resistance ($R_s$) of the structure, the nature of Schottky barrier height (SBH) and their homogeneities, doping concentration, applied frequency and temperature, electric field and polarization processes [8,9].

Both the frequency and temperature are more effective on the electrical and dielectric properties of the electronic devices. At low temperatures, these devices aren't enough free charges and many of them may be frozen. When the temperature becomes increases, more and more carriers electron or holes can be passed on the top of barrier height and so yield an excess capacitance and conductance to measure of them [9–12]. Similarly, at low frequencies surface states can easy follow the alternating signal and yield an excess capacitance and conductance to measure of them. The native or deposited interlayer can be caused easy polarized under an external electric field that displaces the charges from their equilibrium position or traps. Although there are many experimental studies of these structure parameters such as $\Phi_{Bo}$ and n but, there has been no consensus especially on their formation of BH and interfacial layer at M/S interface and current-transport/conduction mechanism (CCMs or CTMs) yet [9,10]. The impedance-voltage (*Z-V*) and conductance-voltage (*I-V*) properties could not be determined by measurements at a single temperature and frequency. On the contrary, the measurements should be carried out over a large frequency range at a constant temperature or vice versa, in order to get more

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information on CCMs, polarization processes and dielectric properties [9–12]. Chand and Kumar [12] investigated *I-V-T* characteristics of $Pd_2Si$/n-Si Schottky barrier diodes in wide temperature range and reported that the basis of TE theory reveals a decrease in the value of $n$ and an increase in $\Phi_{Bo}$ with increasing temperature. Such a behavior of BH is in agreement with the negative temperature coefficient of BH or forbidden bandgap semiconductor ($\alpha = -\Delta Eg/\Delta T$) in ideal SBDs. The high value of n and low value of BH are evident in the deviation of TE theory. Therefore, the high value of n in these devices can be explained by the effects of the voltage drop on over the interlayer, $N_{ss}$, effective BH *(Φe),* ideality factor ($n$) and barrier inhomogeneity between the metal and the semiconductor. Card and Rhoderick [13] reported that the obtained high values of n can be attributed to the image-force lowering effect, generation-recombination (GR), the existence of many low barriers or patches at around mean BH between Au and n-Si and tunneling through the barrier. Therefore, such barrier inhomogeneity leads to an increase in $n$.

ZnO has been used in different applications for many years due to its superior properties such as high thermal/chemical stability, radiation resistant, non-toxicity, wide band gap (~3.4 eV) and high exciton binding energy (~60 meV) [14–17]. In addition, ZnO has nanostructure with natively doped semiconductors due to zinc interstitials. These vacancies give a low resistance, large breakdown voltages, low background and operability at high temperatures. Due to these excellent properties, ZnO is used in many application areas such as photonic, electronic, UV light emitted detectors (UVLEDs), solar cells (SCs) and chemical sensors [17,18]. In recent years, MS type structures with ZnO interface layer have been produced and studied by many researchers in different ways [8,16–20]. Asghar et al. [8] fabricated Au/ZnO/Si Schottky diods and characterized temperature dependent *I-V* and *C-V* measurements between 150 and 400 K. They reported that the ideality factor decreased and barrier height increased with increasing temperature. They also observed a deep defect with 0.57 eV activation energy below the conduction band. Aydoğan et al. [19] fabricated Au/ZnO/n-Si by electrochemical deposition method and measured capacitance–voltage-frequency (*C–V-f*) characteristics of the structure at the room temperature. They saw that the prevailing transport mechanism at large forward bias is the trap-filled space charge-limited current. In addition, they approved that the higher values of capacitance at low frequencies can be attributed to the excess capacitance resulting from the interface states in equilibrium with the ZnO that can follow the alternating current (ac) signal.

In our previous study, Au/ZnO/n-Si structures were investigated as a function of frequency and bias voltage [11] and many important electrical parameters such as concentration of donor atoms ($N_D$), Fermi energy level ($E_F$), $\Phi_B$, and depletion layer width ($W_D$) of the structure were investigated. Additionally in that study, the voltage-dependent profiles of $N_{ss}$ and $R_s$ were obtained from the high-low frequency capacitance and Nicollian-Brews methods. In this study, the effects of $N_{ss}$, $R_s$, interfacial ZnO layer and relaxation process on the dielectric properties of fabricated Au/ZnO/n-Si was identified. Therefore, the values of $\varepsilon^*$, $M^*$ and $\sigma_{ac}$ were investigated in a wide frequency range. In addition, to determine the effect of ZnO interfacial layer on the electrical behavior and the possible CCMs between 80 K and 400 K, the *I-V* plots of the prepared structure were investigated as a function temperature and voltage.

## 2. Experimental details

Au/ZnO/n-Si (MIS) devices/structures were prepared on float-zone n-Si (Phosphour -doped) wafer which has $^{<}100^{>}$ orientation, 400 μm thickness and 0.1 Ω cm resistance. Firstly, Si wafer was degreased for five minutes by acetone trichloroethylene and ethanol in ultrasonic bath. After that, it was etched in a solution of $6HNO_3$:1HF:$35H_2O_2$, 20% HF and quenched in deionized water (18 MΩ cm) for 5 min. After this cleaning procedure, high purity gold (99.999%) with a thickness of ~1500 Å was thermally evaporated on the back side of n-Si at about $2 \times 10^{-6}$ Torr in metal evaporation system (MES). Then, n-Si/Au was tempered at 500 °C for 30 min under flowing dry $N_2$ atmosphere to obviate oxidation of n-Si surface for obtaining low resistance back contact. Zinc oxide thin film was deposited on the uncoated surface of n-Si wafer by using RF sputtering technique at about 30 mTorr. The thickness of ZnO layer ($d_i$) was measured as 30 nm by profile-meter. After the formation of ZnO layer, ultra-pure Au was evaporated on the ZnO layer in the same system with 0.0314 $cm^{-2}$ areas and 150 nm thickness (Fig. 1). The thickness and the deposition rates of the Au layer were controlled by a quartz crystal thickness meter.

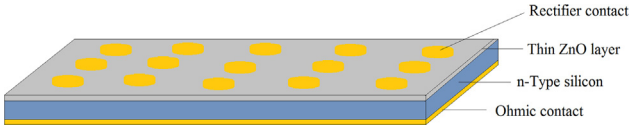


**Fig. 1.** The schematic of Au/ZnO/n-Si structure.

To apply electrical measurements, the fabricated Au/ZnO/n-Si structure was mounted on a Cupper holder by using a silver paste. The upper electrodes were made from the Schottky contacts by using a Cu-wires with the help of silver paste. The impedance measurements were applied in a wide frequency range (700 Hz-1 MHz) and voltage (−6V-(6 V)) at the room temperature by using a HP4192A-LF impedance analyzer. In addition the forward and reverse bias *I-V-T* measurements were performed by using a HP-2400 computerized source-meters in the temperature and voltage ranges of 80–400 K and ± 2 V, respectively. These measurements were performed in the JANES-VPF475 cryostat at about $2 \times 10^{-3}$ Torr using IEEE-488 AC/DC converter card.

## 3. Experimental results

### 3.1. Morphological analyses of ZnO deposited

The surface morphologies of ZnO film forming on n-Si substrate, disclose the crystallinity and crystallite sizes of them by using scanning-electron microscopy (SEM) and atomic-force microscopy (AFM) images (Fig. 2a-c). The application of AFM at 3–3 μm surface area was assessed using the non-contact mode AFM. As seen in Fig. 2a-c, the deposited film was uniform, crack-free and well coated on the substrate surface. By comparing AFM images with SEM images, it is noticed that the surface has same smoothness and same crystallite size. The mean grain size of ZnO film was obtained as 15.2 nm from AFM and 22.6 nm from SEM images was calculated by Imagej program. The root mean square (RMS) and average roughness values of the sample were obtained from the AFM images as 0.66 nm and 0.53 nm respectively. These values indicate that the coated film surface is quietly sleek and smooth.

### 3.2. Dielectric properties of Au/ZnO/n-Si structures

The real and imaginary components of $\varepsilon^*$, $M^*$, tan$\delta$ and $\sigma$ values have been study by using the values of $C$ and $G$ data for Au/ZnO/n-Si structure in the wide frequency range (700 Hz-1 MHz) at the room temperature. The complex permittivity formalism of a (MIS) and (MOS) structures with a thin interfacial layer can be defined as [21,22]:

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = (C_m/C_o) - j(G_m/\omega C_o) \quad (1)$$

Where, $j$ is the imaginary root of $-1$, $C_m$ and $G_m$ are the measured $C$ and $G/w$ and $\omega$ is the angular frequency. $C_o$ is the capacitance of an empty capacitor and it can be computed from the rectifier contact area ($A$), the space permittivity ($\varepsilon_o = 8.85 \times 10^{-14}$ F/cm) and interfacial layer thickness ($d_i$) can be defined from

$$C_o = \varepsilon_o A/d_i \quad (2)$$

The value of dielectric loss tangent ($tan\ \delta$) can also be computed by using $\varepsilon'$ and $\varepsilon''$values as follows [21,23,24]: