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Optimisation of pH of the $CdCl_2$ + $Ga_2(SO_4)_3$ activation step of CdS/CdTe based Thin-Film solar cells

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ABSTRACT

In order to produce high efficiency solar cells based on CdTe, $CdCl_2$ post-growth treatment is an essential processing step. This treatment can be further improved by adding elements such as Fluorine and Gallium into the $CdCl_2$ solution. Through systematic experimentation, it has been found that the pH value of the treatment solution also affect the conversion efficiency of the solar cells. This work therefore focuses on the effect of pH value of $CdCl_2$ + $Ga_2(SO_4)_3$ aqueous solution on the device efficiencies. The graded bandgap device structure, glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au was used in this work. The pH values of 1.00, 2.00 and 3.00 for $CdCl_2$ + $Ga_2(SO_4)_3$ solutions were utilised for the activation of glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers and its effects were explored for both the CdTe material and device properties. It has been found that both CdTe material properties and solar cell device properties are superior when the pH value of 2.00 is used for post-growth treatment. The best conversion efficiency observed in this work for the above graded bandgap device is 12.2%.

1. Introduction

Tellurium (Te) precipitation in cadmium telluride (CdTe) has been a known issue in CdTe layers irrespective of the growth technique (Fernández, 2003). An integral part of achieving a reduction in Te precipitation and highly efficient solar cells has been dependent on the post-growth treatment (PGT) of CdTe in the presence of excess Cd, chlorine (Dharmadasa, 2014) and fluorine (Rios-Flores et al., 2012) ($CdCl_2$ treatment). Amongst the advantages associated with PGT includes the improvement in grain growth, recrystallisation, optical property, electrical conductivity, doping concentration, grain boundary passivation, improved Cd/Te composition, CdS/CdTe interface morphology (Basol, 1992; Bosio et al., 2006; Dharmadasa et al., 2017; Liu et al., 2015; Xue et al., 2016) and reduction in native defects (Dharmadasa et al., 2015a,b). Different post-growth treatments have been utilised for the improvement of the characteristic properties of CdTe as documented in the literature (Major et al., 2016, 2015; Mis-Fernández et al., 2017; Williams et al., 2015). Based on the ability of gallium to dissolve Te-precipitates in CdTe (Fernández, 2003; Sochinskii et al., 1993), our previous research work has been focused on its incorporation in the usual $CdCl_2$ treatment of CdTe (Ojo et al., 2017; Olusola et al., 2017) from which high-efficiency CdS/CdTe-based devices were fabricated with improved material and electronic properties. So far, the effect of pH on the $CdCl_2$ + $Ga_2(SO_4)_3$ (GCT) post-growth treatment of CdS/CdTe based solar cell is yet unknown. In the present study, the focus was on the effect of pH on the $CdCl_2$ + $Ga_2(SO_4)_3$ PGT with the aim to further improve both the material and electronic properties of glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices fabricated.

2. Experimental details

All the chemicals and glass/FTO substrates utilised in this sets of experiments were bought from Sigma Aldrich UK. Two-electrode electroplating technique was employed for all the deposited semiconductors utilised in this work in which a high purity graphite electrode is the anode, and transparent conducting oxide (TCO) was used as the cathode. The specification of the glass/fluorine-doped tin oxide (FTO) utilised in this work is TEC-7 with a sheet resistance of ~7 Ω/□. Prior to the electroplating, the glass/FTO substrates were cut into 4 × 3 cm^2, ultrasonically washed for 15 min in soap water, rinsed in deionised (DI) water, degreased using acetone and rinsed afterwards in a flow of DI water. Before the transfer of the glass/FTO into the electrolytic bath, the substrate is attached to a high purity graphite rod using polytetrafluoroethylene (PTFE) tape but only the FTO surface was in contact with the electrolyte. A computerised GillAC potentiostat was utilised as the power supply source.

2.1. Sample preparation

The *n*-ZnS buffer layer was electrodeposited (ED) on the glass/FTO

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substrates from an electrolyte containing zinc sulphate monohydrate ($ZnSO_4{\cdot}H_2O$) and ammonium thiosulphate ($(NH_4)_2S_2O_3$) with respective purity of 99.9% and 98%. The electrolytic bath was prepared by mixing 0.2 M $ZnSO_4{\cdot}H_2O$ and 0.2 M $(NH_4)_2S_2O_3$ aqueous solutions in 400 ml plastic vessel to use as zinc and sulphur precursors respectively. For this work, 50 nm thick *n*-ZnS layers were electroplated at a cathodic voltage of 1425 mV close to the *p*-to-*n* conduction type transition voltage (V_i). Details of the ED-ZnS has been documented in the literature (Madugu et al., 2016). The electrodeposited glass/FTO/*n*-ZnS layers were annealed in air at 300 °C and air-cooled afterwards. It should be noted that the conduction type of the *n*-ZnS is retained after annealing (Madugu et al., 2016).

65 nm thick *n*-CdS window layers were electroplated on the post-growth treated glass/FTO/*n*-ZnS layers. The CdS was electroplated from an aqueous electrolyte containing 0.3 M hydrated cadmium chloride ($CdCl_2{\cdot}xH_2O$) and 0.03 M ammonium thiosulphate ($(NH_4)_2S_2O_3$) with respective purity of 99.99% and 98% in 400 ml of DI water. The CdS layers were deposited at a pre-optimised cathodic voltage of 1200 mV (Abdul-Manaf et al., 2015). The deposited glass/FTO/*n*-ZnS/*n*-CdS structure was annealed in the presence of $CdCl_2$. The $CdCl_2$ treatment was performed by adding few drops of aqueous solution containing 0.1 M $CdCl_2$ in 20 ml of DI water to the surface of the semiconductor layer. The full coverage of the layers with the treatment solutions was achieved by spreading the solution using solution-damped cotton bud. The semiconductor layer was allowed to air-dry and heat treated at 400 °C for 20 min. The treated glass/FTO/*n*-ZnS/*n*-CdS layers were air-cooled and rinsed in DI water before *n*-CdTe layer deposition. Full details of deposition and optimisation of ED-CdS layer has been published in the literature (Abdul-Manaf et al., 2015). It should be noted that CdS layers are intrinsically *n*-type due defects related to Cd interstitials and S vacancies in CdS layers (Sathaye and Sinha, 1976).

1150 nm thick *n*-CdTe layers were electrodeposited at 1400 mV on the glass/FTO/*n*-ZnS/*n*-CdS substrate. The CdTe layers were deposited from an electrolyte containing 1.5 M cadmium nitrate tetrahydrate ($Cd(NO_3)_2{\cdot}4H_2O$) and 0.0023 M tellurium dioxide (TeO_2) with respective purity of 99.0% and 99.99% in 400 ml of deionised water. Full details of deposition, characterisation and optimisation of the electroplated CdTe layers has been documented in the literature (Salim et al., 2015). Prior to GCT activation process of the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe, the $4 \times 3\ cm^2$ glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were cut into 3 sets of $4 \times 1\ cm^2$ samples.

The $CdCl_2 + Ga_2(SO_4)_3$ solution utilised for the GCT was prepared in aqueous solution containing 0.1 M $CdCl_2$ and 0.05 M $Ga_2(SO_4)_3$ in a 60 ml of DI water. The solution was stirred for 60 min to achieve homogeneity and 20 ml of the solution was poured into three different 25 ml glass beakers. The pH of the $CdCl_2 + Ga_2(SO_4)_3$ solutions were adjusted to 1.00 ± 0.02, 2.00 ± 0.02 and 3.00 ± 0.02 using dilute HCl solution. Afterwards, the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were treated using $CdCl_2 + Ga_2(SO_4)_3$ solutions of different pH, dried in air and heat treated at 400 °C for 20 min in air atmosphere (Ojo et al., 2017). The full coverage of the layers was achieved by the use of solution damped cotton buds.

The annealed glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were etched using aqueous solutions containing H_2SO_4 and $K_2Cr_2O_7$ for acid etching, and NaOH and $Na_2S_2O_3$ for alkaline etching for 2 s and 2 min respectively to improve the metal/semiconductor contact (Dharmadasa et al., 1998). The glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were immediately transferred to a high vacuum system to deposit 100 nm thick Au contacts of 2 mm diameter on the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe structure at a low pressure of $10^{-5}\ Nm^{-2}$.

2.2. Graded bandgap configuration

The basic concept behind graded bandgap (GBG) solar cell is the possibility of effective harnessing of photons across the ultraviolet (UV), visible (Vis) and infrared (IR) regions (Dharmadasa, 2005). This concept has been validated in the literature across organic (Ergen et al., 2016), inorganic (Dharmadasa et al., 2011; Dharmadasa et al., 2015a,b) and hybrid (Dharmadasa, 2005; Ergen et al., 2016) solar cell technology. Graded bandgap can be achieved by grading the semiconductor layers in such a way that the bandgap varies throughout the entire thickness (Dharmadasa et al., 2011). GBG can also be produced by successively growing semiconductor materials on top of each other in which the layers are arranged such that the bandgap decreases gradually while the conductivity type gradually changes from one type to the other (Dharmadasa, 2005).

The earliest work that theoretically described the functionality of GBG configuration was reported by Tauc (1957). His work elucidates the possibility of GBG solar cell configuration attaining higher conversion efficiency above the well-explored *p*-*n* junction cells stimulated interest in the photovoltaic research community. Taking into consideration the photogenerated current, it was proven theoretically that GBG solar cell configurations are capable of attaining a conversion efficiency of ~38% under AM1.5 (Emtage, 1962; Wolf, 1960) as compared to the 23% of single *p*-*n* junction solar cells. Based on this theoretical understanding, the first sets of graded bandgap cells were fabricated and reported in the 1970 s (Hovel and Woodall, 1973; Konagai and Takahashi, 1975) by gradual doping of only *p*-type gallium arsenide (GaAs) with aluminium. The published work demonstrated a single-sided *p*-type grading of *p*-$Ga_{1-x}Al_xAs$/*n*-GaAs solar cell. In 2002, the first model of full solar cell device bandgap grading was proposed and published by Dharmadasa et al. (Dharmadasa et al., 2002). The full graded bandgap (GBG) architectures as proposed in the literature (Dharmadasa et al., 2005; Dharmadasa, 2005) can be accomplished by the incorporation of either an *n*-type or *p*-type wide bandgap front-layer with a steady reduction in bandgap towards *p*-type or *n*-type back layer respectively.

The glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au graded bandgap configuration examined in this work (see Fig. 1) is relative to the technology as documented in the literature (Dharmadasa et al., 2005). It should be noted that the incorporated semiconductor layers (ZnS, CdS, and CdTe) have been individually examined and documented in the literature (Abdul-Manaf et al., 2015; Madugu et al., 2016; Salim et al., 2015). Asides from the bandgap grading of ZnS (3.72 eV (Madugu et al., 2016)), CdS (2.42 eV (Abdul-Manaf et al., 2015)), and CdTe (1.50 eV (Salim et al., 2015)), there are possible formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} ternary compounds in-between successively deposited semiconductor layers due to interface interaction and chemical reactions. Literature on bandgap grading based on incorporated ZnS/CdS/CdTe layers have been well established in the literature (Han et al.,

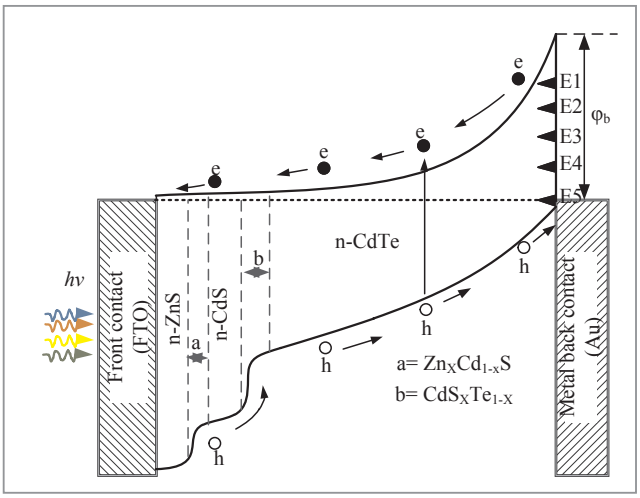

Fig. 1. A typical band diagram of graded bandgap glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device configuration.