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Low-cost and low-temperature chemical oxide passivation process for large area single crystalline silicon solar cells

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ABSTRACT

Although thermally grown silicon dioxide is an excellent surface passivation layer for Si wafers, its industrial applicability for solar cell surface passivation is limited due to low throughput and high cost. This has prompted the exploration of low temperature and chemical silicon dioxide processes for silicon solar cells. In this work, a low-cost, low-temperature (40 °C), non-acidic and safe chemical oxide passivation process (named as NCPRE-oxide) with only sodium hypochlorite (NaOCl) solution is proposed and investigated on large area wafers (125 mm × 125 mm). This process uses a single-component chemical solution to grow ultra-thin silicon oxide (SiO_x) layer of thickness of about 1.5 nm. The chemical SiO_x layer capped with hydrogenated amorphous silicon nitride (SiN_x:H) improves passivation on the n-type silicon surface. A considerable enhancement in the effective minority carrier lifetime (τ_{eff}) is observed for SiN_x:H/SiO_x stack on the phosphorous diffused pyramidal textured silicon surface. The versatility of the NCPRE-oxide is verified by transmission electron microscopy, ellipsometry, X-ray photoelectron spectroscopy, effective minority carrier lifetime and photoluminescence imaging measurements. The introduction of present SiN_x:H/SiO_x stack in our baseline cell fabrication process resulted in the improvement in cell efficiency by 0.3% (absolute) for screen-printed full area aluminum back surface field cells.

1. Introduction

Crystalline silicon (c-Si) solar cell technology is presently dominating the global photovoltaic (PV) market with a share of above 90% (ITRPV, 2017) due to the persistent improvements in performance and reduction in the cost of materials and processes used in the production of solar cells. Evolution of Si solar cell technology from aluminum-back surface field (Al-BSF: the most prominent technology at present) structure to high-performance interdigitated back contact (IBC) and heterojunction with intrinsic thin-layer (HIT) structure is enabled by advances in surface passivation techniques.

A passivation layer can reduce the surface recombination losses by minimizing the surface states density by saturating the dangling bonds and this type of passivation is called chemical passivation. Passivation can be also achieved by introducing a surface field that would repel one type of the carrier and this is called field-effect passivation (Aberle, 2000; Mandelkorn and Lamneck, 1990). In silicon solar cells, different schemes are used to passivate the surfaces such as thermal silicon dioxide (SiO_2) (Gruenbaum et al., 1990; Stephens et al., 1994; Glunz et al., 1994), hydrogenated amorphous silicon nitride (SiN_x:H) (Rohatgi et al., 2000; Aberle, 2001; Lauinger et al., 1995), hydrogenated amorphous silicon (Jeon et al., 2010; Ge et al., 2012), high-low junctions (Aberle, 2000; Blakers and Green, 1986), and p-n junctions (Aberle, 2000).

The thermally grown SiO_2 is an excellent surface passivation layer for both n-type and p-type high resistivity wafers (Aberle, 2000). However, thermal oxidation at high temperature (~1000 °C) can cause severe bulk lifetime degradation, especially in multi-crystalline silicon wafers. The thermally grown oxide has limited industrial applicability due to low throughput and high cost (Aberle, 2000).

SiN_x:H is most commonly used for the passivation of the n^+ emitter layer in n^+-p-p^+ structured conventional Al-BSF Si solar cells. Additionally, it acts as an anti-reflection coating (ARC) to reduce optical losses. It is already well known in the literature that a thin SiO_x layer capped with SiN_x:H layer provides good passivation in high-efficiency solar cells (Duttagupta et al., 2014; Dingemans et al., 2011; Bordihn et al., 2011; Hofmann et al., 2009; Mihailetchi et al., 2008; Glunz, 2007). For industrial applications, low temperature and low cost methods have been investigated by various researchers such as low-temperature thermal oxidation (Yadav et al., 2017), nitric acid (HNO_3) oxidation of silicon (Mihailetchi et al., 2008; Kobayashi et al., 2010; Bordihn et al., 2011), UV-light excited O_3 oxidation (Tosaka et al.,

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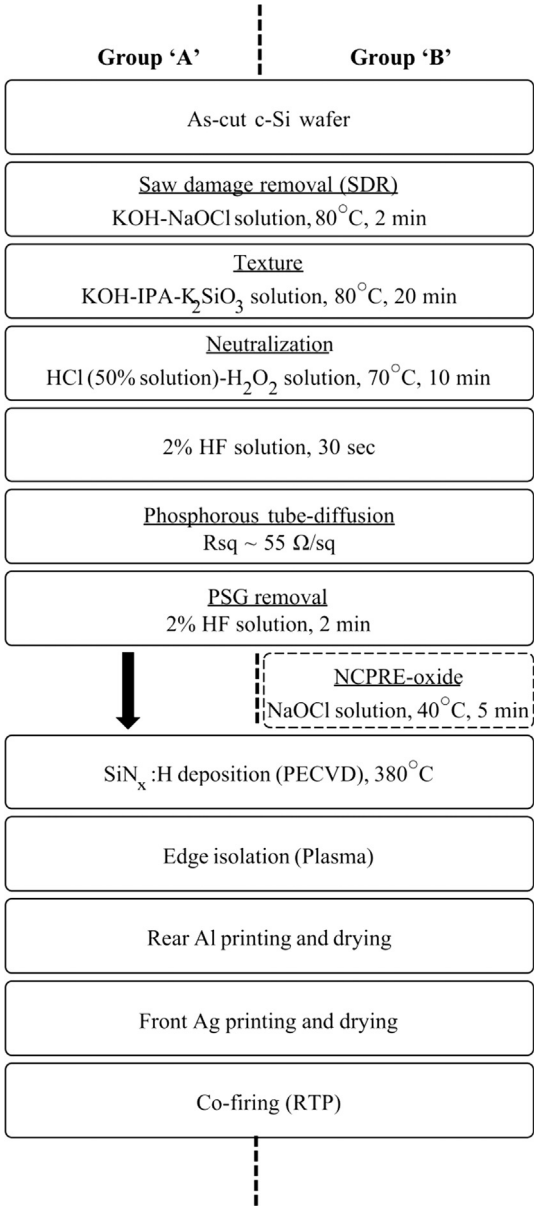

Fig. 1. Process flow of solar cell fabrication with SiN_X:H layer (group 'A') and SiN_X:H/SiO_X (NCPRE-oxide) stack (group 'B'). NCPRE-oxide process step is shown as a dashed line box.

2005), UV-Ozone method (UV/O_3) and ozonized DI-water (DIO_3) (Moldovan et al., 2014) to grow thin oxide on Si wafers.

Kobayashi Asuha et al. (2003), Kobayashi et al. (2010) and Mihailetchi et al. (2008) demonstrated that concentrated (68 wt%) HNO_3 at 121 °C can be used as an oxidizing chemical to grow ultra-thin (~1.5 nm) SiO_x layer. Tosaka et al. (2005) have shown oxidation of Si wafer using the UV-light excited O_3 oxidation method. Using this method, a SiO_2 film of a thickness of ~3.6 nm was grown in the temperature range of 70–300 °C in a vacuum chamber at a base pressure of 10^{-3} Pa on 12 mm × 12 mm silicon wafer in 10 min. Moldovan et al. (2014) have shown DIO_3 and UV/O_3 methods to grow tunnel oxide layer for tunnel oxide passivated contact (TOPCon) structure. However, all these chemical oxidation processes either require special care in handling chemicals at high temperature (~100 °C) or costly O_3 generator. Besides, safety issues are also associated with the handling of corrosive acids, UV exposure, O_3, etc. This adds to the cost of implementation for industrial processing.

Sodium hypochlorite solution (NaOCl) had been used as a texturization solution earlier (Gangopadhyay et al., 2005; Basu et al., 2013b). In this work, a low-cost, low-temperature, non-acidic, and safe chemical oxide passivation process is investigated on large area wafers (125 mm × 125 mm). This chemical oxide growth process is referred to as NCPRE-oxide process in the rest of this manuscript. This process uses NaOCl to grow an ultra-thin SiO_x layer on the Si surface. Due to a single component chemical process, the solution is homogeneous which helps in uniform growth of a SiO_x layer on silicon. Our results establish that when this layer is capped with PECVD SiN_x:H, surface passivation improves, and resulted in an enhancement in the effective minority carrier lifetime (τ_{eff}) on pyramidal textured Si surface. This translated to an open circuit voltage (V_{oc}) improvement of 4 mV and an absolute efficiency improvement (η) of 0.3%.

2. Experimental methods

2.1. NCPRE-oxide growth and cell fabrication

In this work, pseudo-square (125 mm × 125 mm), Cz, p-type (boron doped), industrial grade monocrystalline silicon (c-Si) wafers (bulk resistivity of ~2 Ω-cm, ~180 μm thickness, and (1 0 0) surface orientation) were used. Solar cells were fabricated in two groups using process sequences shown in Fig. 1. Pre-cleaning and damage removal process of the wafers prior to texturing was performed simultaneously with potassium hydroxide (KOH) and NaOCl solution (Basu et al., 2010). In this two minutes process at 80 °C, approximately 3 μm of Si was removed from both sides of the wafers. For pyramid formation, a solution containing KOH concentration of 2.5 wt%, 9 ml of potassium silicate (K_2SiO_3) and 300 ml of isopropyl alcohol (IPA) was used in a 6-litre chemical bath. The texturing solution temperature was maintained at a constant value of 80 °C for 20 min for all the processes (Basu et al., 2013a). All textured wafers underwent phosphorous diffusion for a target sheet resistance (R_{sq}) value of 55 Ω/sq. The diffusion was performed in a tube furnace (Protemp USA, *Sirius PRO 200*) using phosphorus oxychloride ($POCl_3$) as the dopant source at 830 °C peak diffusion temperature followed by phosphosilicate glass (PSG) removal in dilute HF. Then wafers were split into two groups: group 'A' and group 'B'. The group 'A' underwent SiN_x:H deposition by plasma-enhanced chemical vapor deposition (PECVD) process in a capacitively coupled plasma system (Oxford Instruments, Plasmalab System 100) at 380 °C. The deposited SiN_x:H film has a refractive index (RI) of 2.0 and thickness of 95 nm as measured on a test sample of polished Si wafer. While group 'B' were treated with hot NaOCl solution (40 °C) for five minutes in a 6-litre chemical bath to grow an ultra-thin silicon oxide (SiO_x) (Yadav et al., 2017). The thickness of this oxide was determined using ellipsometry. Since the thickness obtained is in the same range as that of native oxide, the wafers used for lifetime determination and cell fabrication were transferred to the PECVD system load lock immediately after the oxide growth. The NCPRE-oxide growth process step is shown as dashed line box in Fig. 1. Then, similar SiN_x:H layer deposition process as mentioned for group 'A' was carried out on these wafers, which formed a SiN_x:H/SiO_x stack. After dielectric deposition, all the wafers from both the groups (excluding representative lifetime samples) underwent plasma edge isolation (BSET EQ, NT-2). For screen printed metallization, aluminum (Al) paste (Monocrystal, PASE-1207) and silver (Ag) paste (Dupont, PV19B) were used for the rear and the front contacts, respectively. Cells were printed with a screen printer (Haiku Tech, P200S) and co-fired in a rapid thermal processing (RTP) unit (Allwin21 Corp., AW 610).

2.2. Lifetime sample fabrication

Symmetrical lifetime test structures were fabricated using the representative wafers from both the groups. After symmetrical tube diffusions on both sides of c-Si wafers, the representative wafers