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Development and prospects of surface passivation schemes for high-efficiency c-Si solar cells

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ABSTRACT

Photovoltaic (PV) electric power generation has the potential to account for a major portion of power generation in the global power market. Currently, the PV market is dominated by crystalline silicon (c-Si) solar cells which accounts for more than 80% of the share. Lower cost, optimized process parameters and improved PV cell efficiencies are required to reduce the overall cost per watt peak (W). In this regard, PV cell manufacturers are currently adopting thinner wafers, which tends to increase the surface recombination velocity (SRV). Excellent surface passivation at the front and rear of the PV cell becomes imperative for realizing superior efficienciy on c-Si substrates. In this article, our focus is to discuss the role of the surface passivation process for improving the PV cell efficiency. The fundamentals and strategies to improve the surface passivation for c-Si solar cells are discussed. Surface passivation schemes and materials with the ability to offer field effect passivation with dielectric charges (positive/negative) present in the passivation films were reviewed. Moreover, we discuss the use of a thin-dielectric passivation layer with a properly selected work function and band offsets for tunneling contacts, facilitating a higher efficiency potential. Finaly, the front/rear surface passivation schemes required for thinner wafers to maintain higher bulk lifetime and higher efficiencies for c-Si solar cells are presented.

1. Introduction

The photovoltaic (PV) market has been rapidly increasing globally in recent years. The cost per watt peak (W) of solar cell modules is the most important parameter for manufacturers, as competition in the PV market is on the rise. Therefore, most manufacturers are currently focusing on optimizing the solar cell processes, which may help in achieving higher efficiencies without increasing the processing cost significantly. Processes such as improving the surface structuring and texturization considerably enhance the light trapping ability of the devices (Quiebras, 2013). In addition, the emitter profile distribution with selective doping enhances the solar cell efficiency (Rahman, 2012). The formation of thinner contacts with lower shading loss and excellent electrical properties is an important parameter for the achievement of higher efficiency (Rehman and Lee, 2014). Moreover, the passivation layers on the front and rear surface help to reduce the recombination losses and enhances the solar cell performance significantly (Balaji et al., 2015).

The surface passivation of crystalline silicon (c-Si) has remarkable significance for PV applications. Eventually, high-efficiency c-Si solar cells require an excellent level of surface passivation. In recent times, the surface passivation has become more important owing to the cost-driven reduction of the thickness for conventional c-Si solar cells. Silicon-dioxide (SiO) grown by oxidation process at higher temperatures (≥ 900 °C) were used to suppress surface recombination effectively with superior efficiencies for c-Si solar cells on the laboratory scale (Green et al., 1990; A, 1990; Zhao et al., 2001). By using a combination of thermally grown SiO with evaporated Al and additional annealing treatment at about 400 °C (anneal process), the surface recombination velocities (SRVs) were reduced to values below 20 cm/s on p-type substrates (Kerr and Cuevas, 2001). This SiO/Al layers stacked on the rear side also enables an opportunity to improve the light trapping properties of the cell by acting as an excellent for near bandgap photons and hence provides the short-circuit current of the cell. Despite the fact that SiO offers excellent surface passivation quality, its implementation on an industrial scale is limited as the high temperature

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processes are detrimental to silicon bulk lifetime. In particular, high thermal processes (above 900 °C), usually significantly degrades the bulk lifetimes, specifically for multi-crystalline silicon wafers (Stocks et al., 1997). Low temperature alternates offering surface passivation properties that are comparable to that of annealed SiO are required for future industrial based high-efficiency crystalline silicon solar cells. The use of silicon nitride (SiN) grown by plasma-enhanced chemical vapor deposition (PECVD) at ∼400 °C has been reported as an alternative with comparably low SRVs as alnealed SiO on p-type substrates (Lauinger et al., 1996; Schmidt et al., 2008). However, the SiN deposition on the rear side of the passivated emitter and rear cell (PERC) type solar cells resulted in significantly reduced short-current density compared to silicon dioxide counterparts (Dauwe et al., 2003). This is because silicon nitride has a large density of positive charges inside the silicon nitride layer; this tends to induce an inversion layer in Si below the silicon nitride later, which has a detrimental effect that is known as "parasitic shunting" when coupled with base contact and causes significant loss in short-circuit current density (Dauwe et al., 2002). Apart from that, other materials such as amorphous silicon (a-Si), stacks of a-Si/SiO, and aluminium oxide (AlO) have been used to passivate the rear surface of the cell effectively (Rahman and Khan, 2012). Among them, low temperature growth of AlO by atomic layer deposition (ALD), provides an excellent level of surface passivation, which is confirmed from carrier lifetime measurements on n- and p-type silicon substrates (Rahman and Khan, 2012; Hoex et al., 2006; Schmidt et al., 2008).

Surface passivation on both the front- and rear-sides of the PV cells is the basic requirement to achieve higher efficiencies. In this regard, electrical surface passivation tends to play a vital role in describing the conversion efficiency as well as the fabrication cost of crystalline based silicon PV cells. Highly stable PV modules (life span of more than 20 years) require the passivation techniques with lower thermal budget (≤400 °C) to be developed on industrial scale. In this article, our focus is to discuss the details of the development as well as the potential of surface passivation schemes for high-efficiency c-Si solar cells.

2. Fundamentals of surface passivation

The silicon surface represents the largest possible discontinuity of the symmetry of the crystal lattice. This discontinuity is owing to the presence of a large number of partially bonded silicon atoms (limited electron pairing of the atoms at the surface). These unpaired electrons tend to create a large density of defects (surface states) within the bandgap existing at the semiconductor surface. These defect levels tend to enhance the recombination rates at the surface.

The Schockley-Read-Hall (SRH) theory describes the recombination by defect states in semiconductors. The SRH theory extracts the rate of surface recombination $U_{surface}$ for a single defect located at an energy E_t (trap energy level) Rein (2006).

$$U_s = \frac{n_s p_s - n_i^2}{\tau_{p0}(n_s + n_1) + \tau_{n0}(p_s + p_1)} \tag{1}$$

Here, n_s and p_s are electrons and holes concentrations at the surface, respectively. τ_{n0} and τ_{p0} represent the capture time constants of electrons and holes. These capture time constants are related to defect concentrations (N_t), capture cross-sections (σ_n) and (σ_p), and thermal velocity (v_{th}) of the specific defect center. n and p are statistical parameters expressed as a function of the intrinsic Fermi level (E_i).

$$\tau_{p0} = [N_t \sigma_p v_{th}]^{-1}, \tau_{n0} = [N_t \sigma_n v_{th}]^{-1}$$

$$n_1 \equiv n_i exp^{\left(\frac{E_t - E_i}{kT}\right)}, p_1 \equiv n_i exp^{\left(\frac{E_t - E_i}{kT}\right)}, n_1 p_1 = n_i^2$$

This surface recombination can also be represented in terms of surface recombination velocity (SRV) parameters for electrons (S_n) and holes (S_p).

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{2}$$

In fact, the defect states do not occupy a single energy level but are distributed across the Si bandgap, and as a result, the defect parameters are not constant. These parameters depend on the energetic location of the defects in the band gap. Thus, extended SRH formalism is required to express the rate of surface recombination ($U_{sarface}$). In Eq. (1), the SRH rate of recombination for single defect can be integrated over the entire bandgap, with interface trap density (D_{it}) as the weighting function. This helps in extracting the overall surface recombination rate (U_s) or the effective surface recombination velocity (S_{eff}).

$$U_s = (n_s p_s - n_i^2) \times \int_{E_v}^{E_c} \frac{v_{th} D_{it}(E_t) dE_t}{[n_s + n_1(E_t)]\sigma_p^1(E_t) + [p_s + p_1(E_t)]\sigma_n^1(E_t)} \tag{3}$$

The surface recombination rate (Us) and excess carrier density (Δ) at the surface give the value of the SRV.

$$S \equiv \frac{U_s}{\Delta n_s} \tag{4}$$

Usually, the Girisch algorithm (Girisch and De Keersmaecker, 1988) is required to calculate the doping and injection dependence of the SRV, and the analytical expression can only be found in the case of the flat band condition. The surface concentrations can be represented by (Δn_s), as under flat band conditions the excess carrier densities of electrons (Δn_s) and holes (Δp_s) are equal under illumination (Aberle, 1999). The flat band condition SRV can be calculated by:

$$S(\Delta n_s) = \frac{n_0 + p_0 + \Delta n_s}{\frac{n_0 + n_1 + \Delta n_s}{S_{p0}} + \frac{p_0 + p_1 + \Delta n_s}{S_{n0}}} \tag{5}$$

This SRV is usually used to quantify the surface recombination processes. Here, n_0 represents electrons and p_0 represents holes of the equilibrium concentration. In general, surface passivation is achieved by reducing the number of interface defect states and by the shielding of electrons (n_s) and holes (p_s) at the c-Si surface by means of a built-in electric field (field-effect passivation). Equation (1) demonstrates this phenomenon, and the term ($n_s p_s - n_i^2$) in the equation is responsible for the deviation of the system from thermal equilibrium. The strategies were employed improve the surface passivation are explained in the next section.

3. Strategies for improving the surface passivation

Two types of strategies are useful to reduce the surface recombination rate or effective SRV (S_{eff}) at semiconductor surface. First, as can be seen from Eq. (1), the density of interface states (D_{it}) at the semiconductor surface directly impacts the SRV. Hence, the reduction in D_{it} (from Eq. (3).) is the most obvious and upfront method for achieving good surface passivation.

Scientifically, the use of appropriate surface passivating materials has the tendency to reduce the concentration of D_{it} at the semiconductor surface. The dangling bonds at the c-Si surface can be cured effectively by hydrogen present in passivating materials. The use of annealing gas containing hydrogen (e.g. foaming gas with 4% hydrogen and 96% argon/N) also passivates these dangling bonds. The use of polar liquids for Si immersion with/without illumination can be used as an alternate method for surface passivation (Yablonovitch et al., 1986; Grant, 2012; Jin et al., 2007). Amorphous silicon, silicon oxides, aluminum oxides and silicon nitrides are the most popular applicants for silicon surface passivation. For example, thermal SiO film with post-annealing process in foaming gas (containing hydrogen), resulted in reduction of $D_{it,midgap}$ to as low as $10^9\ \mathrm{eV}^{-1}\ \mathrm{cm}^{-2}$ for an undiffused c-Si wafer. The reduction in D_{it} and the rate of surface recombination depend largely on the process conditions and post-deposition annealing.