



Optimization of lapping processes of silicon wafer for photovoltaic applications



Savas Ozturk^{a,b,*}, Levent Aydin^c, Nilay Kucukdogan^d, Erdal Celik^e

^a Faculty of Engineering and Architecture, Department of Material Science and Engineering, Izmir Katip Celebi University, 35620 Izmir, Turkey

^b The Graduate School of Natural and Applied Sciences, Dokuz Eylul University, 35370 Izmir, Turkey

^c Faculty of Engineering and Architecture, Department of Mechanical Engineering, Izmir Katip Celebi University, 35620 Izmir, Turkey

^d The Graduate School of Natural And Applied Sciences, Izmir Katip Celebi University, Izmir, Turkey

^e Faculty of Engineering, Department of Metallurgical and Materials Engineering, Dokuz Eylul University, 35370 Izmir, Turkey

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ABSTRACT

The thinning of the silicon wafers and the smoothening of the surface are carried out by grinding and lapping processes. The lapping process is especially preferred to produce less surface damage of the silicon wafer in the production of high-efficiency solar cells. In this process, the surface roughness of the sample is the most influential parameter of pressure, rotation speed, lapping time and solution characteristics. In this study, rotation speed and lapping time were determined as design variables in the lapping processes of wire-sawn silicon wafers of 105 mm in diameter using a lapping and polishing machine. Although there are many studies about surface preparation in lapping process, the studies investigating this issue with theoretical or statistical modeling are very few in the literature. In addition, as a similar engineering process, many studies on the cutting process are available including experimental, modeling and optimization sections, which provides a good realistic design and prediction capability for the phenomenon. A similar study also needs to be done for the lapping process, which is especially preferred for the preparation of the surfaces of sensitive materials. The present study was conducted to fill this gap. In order to optimize the lapping parameters with a success, firstly, multiple nonlinear regression analyzes of experimental data were performed in terms of process parameters. Secondly, optimization studies were carried out based on Differential Evaluation, Nelder-Mead, Random Search and Simulated Annealing algorithms with the proposed regression models. It can be concluded that the present paper introduces significance of collaboration on the surface roughness experimental-modeling-optimization triple in silicon wafer lapping process for photovoltaic applications.

1. Introduction

Solar cells are an energy source that can be easily applied when compared to other renewable energy sources and not a pollutant. Basically, solar cells can be classified as silicon (Si) based, thin film, flexible and organic (Abdelfatah et al., 2015; Lau et al., 2013; Seyhan et al., 2017). Nowadays, silicon-based solar panels (single or multi-crystalline) dominate 80% of the solar panels used in the world (Huang et al., 2017; Kayabasi et al., 2017a). However, the biggest problem of the widespread energy source technology is the cost of producing solar panels in the preparation of silicon substrate materials. Surface smoothing is a very important process step in Si wafer production. As an additional information, the sanding process constitutes 20% of the total wafer production (Hahn, 2001). In silicon-based solar cells, it is known that efficiency is increased by reducing the surface defects (surface

cracks, defects, voids, scratches, etc. are induced during the sawing process and slicing from the ingot) and this process can be achieved by well-organized lapping and polishing process (Amanov et al., 2017; Ozturk et al., 2017).

There are two main types of equipment utilized in wafer surface smoothing process, namely lapping and grinding. Lapping is a surface preparation method to obtain a good surface quality (Konneh et al., 2012). If the lapping is compared to the grinding, it can be seen that the amount of material removal is low. However, there is no heating on the material surface and relatively low forces are applied to the workpiece in the process. This situation also allows the fragile and brittle materials to be worked without damage. The lapping efficiency is influenced by some important process variables such as abrasive grain size, rotation speed, amount and viscosity of lapping compound (Doi et al., 2011). It is not clear how the effects of variables on the process efficiency based

* Corresponding author at: Faculty of Engineering and Architecture, Department of Material Science and Engineering, Izmir Katip Celebi University, 35620 Izmir, Turkey.

E-mail addresses: ozturksavas@gmail.com (S. Ozturk), leventaydinn@gmail.com (L. Aydin), kucukdogan.nilay@gmail.com (N. Kucukdogan), erdal.celik@deu.edu.tr (E. Celik).

on randomness and complexity of the process. Sums of small abrasive grains are carried to the working area by relatively large particles and it is very difficult to establish an analytical approach between rolling and sliding particles. The main reason of this is the constant change in a working environment.

Parametric studies help to recognize and optimize the wafer smoothing conditions. In addition to theoretical analysis, experience-dependent solutions have also been used in surface roughness modeling. The modeling studies based on the process experimental data have been increasing in recent years in the literature. For example, Suwatthikul et al. have investigated the vibration characteristics of lapping process experimentally and damage minimization carried out using Artificial Neural Networks (ANN) (Suwatthikul et al., 2016). Li et al. developed a surface roughness prediction model for shear-thickening polishing using Response Surface Methodology (RSM) (Li et al., 2016). Sun et al. have made a theoretical model of grinding force for a self-rotating grinding process of silicon wafer (Sun et al., 2016). It should be noted that available studies on engineering process modeling generally consider only one or two traditional regression forms. The main issue of the studies is just to obtain a high R^2 value of the model for the experimental study. However, it is not sufficient to describe physical phenomena/engineering process by obtaining a high value of R^2 only. Therefore it is necessary to attempt new lapping process modeling studies including nontraditional regression forms. Moreover, some scientists have also studied both of the modeling and optimization of surface roughness process involving experimental parameters. Recently, in Ozturk et al. an artificial neural network (ANN) simulation was utilized to determine the lapping parameters such as rotation speed, lapping duration and lapping pressure under constant slurry supply for n-type crystalline Silicon (c-Si) wafers (Ozturk et al., 2017).

In the optimization parts of the modeling studies, the stochastic optimization methods (i.e., Artificial Bee Colony (ABC) (Mukherjee et al., 2012; Yusup et al., 2014), Genetic Algorithm (GA) (Durairaj and Gowri, 2013; Mukherjee et al., 2012; Sangwan et al., 2015), Simulated Annealing (Ozturk et al., 2018; Zain et al., 2010), Differential Evolution (Ozturk et al., 2018), Particle Swarm (Hrelja et al., 2014; Raja and Baskar, 2012), Ant Colony (Mukherjee et al., 2012; Raj Mohan and Suresh, 2015), Sheep Flock Optimization (SFO) and Biogeography-Based Optimization (BBO) (Mukherjee et al., 2012)) have been usually preferred for surface roughness minimization problems. However, the investigation of stochastic optimization algorithm applications on surface roughness minimization problems for lapping process is not available in the literature.

In these regards, we introduce a new procedure to obtain more realistic lapping parameters for the minimum surface roughness of Si wafer. First, a detailed study on multiple nonlinear regression analyses including linear, quadratic, trigonometric, logarithmic and their rational forms on the same surface roughness problem has been performed. Secondly, different stochastic optimization algorithms (Differential Evaluation, Nelder-Mead, Random Search and Simulated Annealing) have been utilized systematically to avoid inherent scattering of the stochastic processes. Thanks to the present paper we will also fill a gap corresponding modeling-optimization processes for lapping operations in engineering. It is also an important study for the researches aiming directly increase the product yield in photovoltaic applications.

2. Experimental

The experimental motivation of the present paper mainly based on a detailed literature survey about metallographic surface preparation in Si wafering. It was carried out how to investigate the effects of preparation parameters on the surface roughness of Si wafers. After analyzing the published papers about the flattening process of Si wafer, it is seen that the parameters rotation rate, lapping pressure, abrasive and lapping plate type, and lapping time were determined as the most

Table 1
Cutting parameters used in the experiments.

Process Variable	Factor Levels					
Rotation rate (rpm)	25	50	70			
Time (min)	5	10	15	30	45	60

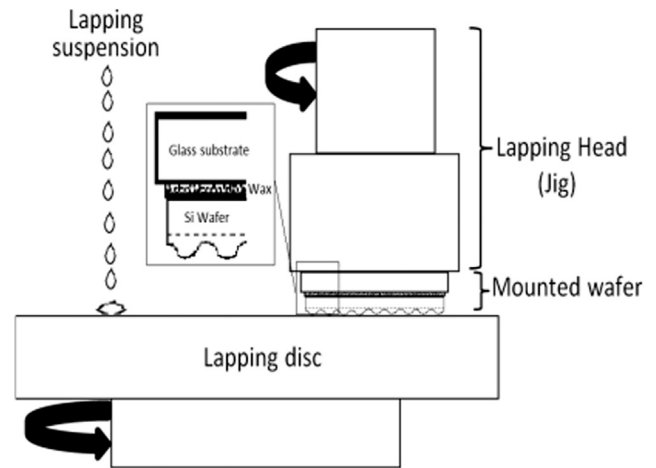


Fig. 1. Schematic drawing of lapping system.

Table 2
Corresponding options for the optimization algorithms DE, NM, RS, and SA.

Options	DE	NM	RS	SA
Cross Over Fractions	0.5	–	–	–
Random Seed	1	5	–	2
Scaling Factor	0.6	–	–	–
Tolerance	0.001	0.001	–	0.001
Contract Ratio	–	0.5	–	–
Expand Ratio	–	2.0	–	–
Reflect Ratio	–	1.0	–	–
Shrink Ratio	–	0.5	–	–
Level Iterations	–	–	–	50
Perturbation Scale	–	–	–	1.0

effective parameters on cutting process for surface roughness (Doi et al., 2011; Kayabasi et al., 2017b). By considering these outcomes, rotation speed and lapping time were determined as effective parameters in the experimental procedure of the present study. All lapping operations were performed under the same conditions. N-type monocrystalline 105 mm diameter Si wafers used in experiments were prepared with the same cutting parameters. Before the lapping process, Si wafers were bonded onto the glass substrate using a binder and once bonded wafer was held on the lapping jig by mean of a vacuum. A general simple factorial design was adopted to the present experiment. Eighteen experimental sets were conducted 5 times and totally 90 wafers were prepared. Lapping operation was performed in Logitech PM5 Lapping and Polishing System with the rotating rate capacity of maximum 70 rotations per minutes (rpm). 0.2–4 kg jig loads applied to sample based on the weight of the jig (8.4 kg) corresponding to the surface area of the samples during the lapping process. Lapping suspension was prepared with water to alumina powder (9 μm) weight ratio of 0.2. The two process parameters and their factor levels are summarized in Table 1. After Si lapping process, a Mitutoyo SJ 210 instrument with 2 μm tip radius at 2.5 mm cutoff length value was used to measure surface roughness (R_a , R_t) of the Si wafers. A microscopic scale stylus profiler (SP) is considered as contact type surface roughness measurement method with electronic amplification. In this process, there are three main steps: (i) contacting of the stylus tip on surface of Si wafers, (ii)

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