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ScienceDirect

Solar Energy 127 (2016) 223–231

SOLAR ENERGY

www.elsevier.com/locate/solener

# Aluminum induced crystallization of amorphous silicon thin films with assistance of electric field for solar photovoltaic applications

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Received 9 November 2015; received in revised form 24 December 2015; accepted 6 January 2016

Communicated by: Associate Editor Gion Calzaferri

**Abstract**

In this current research, the aluminum-induced crystallization of amorphous silicon (a-Si) was studied. Particularly, a-Si film covered with a very thin film of pure aluminum was exposed to a constant electrical voltage and high temperature. Every sample was subjected to annealing for 15 min with the application of an external electrical voltage. Nine treatments of different annealing temperatures and voltages were involved in this research. The levels of annealing temperature were 250 °C, 300 °C, and 350 °C, and the levels of external voltage were of 0 V, 2 V, or 20 V. After the annealing, the electrical, structural, and morphological properties of the a-Si layer have been investigated. Energy dispersive X-ray spectroscopy proved that there is diffusion of aluminum atoms inside the a-Si layer. X-ray diffraction showed that the crystallization depends on both temperatures and external voltage. We also noted that the electrical resistivity decreased significantly with annealing temperature and external voltage increasing. Moreover, the Hall mobility increased sharply with the increasing of annealing temperature and applied voltage, while the carrier concentration deceased slowly with increasing of both of them.


*Keywords:* Amorphous silicon; Crystallization; Annealing; Mobility; Resistivity; Van der Pauw

## 1. Introduction

Silicon (Si) is the eighth most abundant element in the universe. However, it is very rarely found as a free element in nature. Furthermore, Si is the second most abundant element in the Earth's crust (about 28% by mass) after oxygen (Exley, 2009). It is found in sand, soil and rocks, and it is also found in various forms, such as silica (silicon dioxide) and silicates. Over 90% of the Earth's crust is composed of silicate minerals (Wei et al., 2013). In addition, silicon is an essential element in industry, especially electronic manufacturing (Elani et al., 2005; Angermann et al., 2012) and solar photovoltaic technology (Lin and Chiou, 2012; Xia et al., 2011; Yamamoto et al., 2004; Liu et al., 2012; Zhao et al., 2011; Mohamed et al., 2012; Müller et al., 2004; Forbes, 2011; Han et al., 2011).

The crystalline silicon is considered as the most important material in solar-based applications. The crystallization of amorphous silicon (a-Si) thin film and its application has been discussed by many authors, such as

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http://dx.doi.org/10.1016/j.solener.2016.01.035
0038-092X/

(Fuhs et al., 2004; Reber et al., 2004; Toyama and Okamoto, 2006; Yoon et al., 1998; Choi et al., 2000; Kim et al., 2002). For example, Yoon et al. (1998) applied metal induced crystallization (MIC) technique on a-Si covered with 2 nm Ni film using electric field strength of 360 V/cm. They concluded that the solid phase crystallization (SPC) temperature decreases remarkably to below 380 °C in the presence of electrical field. While Choi et al. (2000) studied the thinning of gate insulator in an hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT). They found that the threshold voltage decreases with decreasing gate insulator thickness without changing the field which affects mobility significantly.

Kim et al. (2002) worked on the electric field enhanced crystallization of hydrogenated amorphous silicon (a-Si:H) in contact with nickel catalyst. Specifically, they studied the crystallization kinetics quantitatively, and they concluded that the crystallization rate varies drastically at the electric field of 33 V/cm. They also found that the activation energy for the crystallization is about 85 kJ/mol. Khakifirooz et al. (2001) studied the effect of applied electric field during metal-induced lateral crystallization (MILC) of a-Si in a structure of Ni pads/a Si/Glass, and they observed a lateral growth of 300 μm when annealing at 400 °C for 30 min, while DC voltage of 100 V is applied between Ni silicide pads.

The effect of annealing on a-Si:H at temperature range of 100–300 °C was studied by Haque et al. (1996). They found a dramatic change in the sheet resistance at annealing temperature of 150–250 °C. Moreover, they calculated the electrical properties of annealed a-Si samples at temperatures of 100–300 °C, their results are as follows: The mobility was about 1.4 $cm^2 V^{-1} s^{-1}$ and the resistivity was 0.08–0.13 Ω cm, and the carrier concentration was about $5 \times 10^{15}$ $cm^{-3}$. Nast and Hartmann (2000) studied aluminum-induced crystallization (AIC) of a-Si using various spectroscopy techniques (e.g., X-ray photoelectron spectroscopy), and they concluded that the layer exchange process during AIC of (a-Si) at temperature is lower than the eutectic temperature of Al–Si alloy (577 °C). The growth of crystal silicon on a deposited aluminum was studied by Drüsedau et al. (1998). They found that the effect of Al mediated crystallite growth is related to the existence of a metastable aluminum silicide and diffusion process.

Matsumoto and Yu (2001) prepared a p-type poly silicon from a-Si:H, and they found that the poly-Si could be obtained by annealing of a-Si:H at 450–550 °C for 5–60 min. Furthermore, they obtained a resistivity of 0.06 Ω cm, Hall mobility of 20 $cm^2 V^{-1} s^{-1}$ and carrier concentration of about $10^{18}$ $cm^{-3}$.

Ishikawa et al. (2004) worked on poly-Si silicon thin films prepared by aluminum induced crystallization method. The results show that when the a-Si:H films annealed at temperature range from 350 °C to 550 °C, for 0.5–2 h, the resistivity approached to 1 Ω cm with a carrier concentration of about $10^{18}$ $cm^{-3}$ and mobility of about 10 $cm^2 V^{-1} s^{-1}$.

Furthermore, Fakhar (1999) has also reported that the resistivity for samples annealed at 200–275 °C is about 0.16–0.27 Ω cm. The carrier concentration measures for the same samples were about $3 \times 10^{+19}$ to $2 \times 10^{+20}$ $cm^{-3}$ and the mobility was about 0.26–1.19 $cm^2 V^{-1} s^{-1}$. Choi et al. (2005) studied the mechanism of field – aided lateral crystallization of a-Si. The samples were annealed at temperatures 100–900 °C for 1–13 h. They concluded that the resistivity of the a-Si annealed at 300 °C for 1 h is 500 Ω cm.

In this present work, the effect of the combination of annealing temperature and the applied voltage on electrical and physical properties of amorphous silicon was investigated for the first time. Moreover, the applied temperature is lower than any experiment in the abovementioned references. The motivation of this work is to improve the electrical and physical properties of amorphous silicon for solar photovoltaic application.

## 2. Experimental details

The purpose of this work is to study the physical properties of Al induced crystallization a-Si thin films. The films were deposited on glass substrates, and then annealed while external voltage is applied on the films. DC magnetron sputtering technique was used to deposit 300 nm of amorphous silicon (a-Si) on corning glasses (glass product ID: corning 7059). The shape of the samples was square with 1.25 mm length and 1.25 mm width. A very thin layer of aluminum was sputtered over the a-Si layer. Each sample was secured on a sample holder made from Pyrex. The holder had a connection setup to facilitate the connection to the external voltage during the annealing.

An annealing for 15 min was conducted on each sample individually at a temperature and applied external voltage according to the following levels: The levels of temperature were 250 °C, 300 °C and 350 °C, and the levels of external voltage were 0 V, 2 V and 20 V. Nine different treatments were involved, and 18 samples were treated due to use a second replicate of the experiment. After annealing, the aluminum layer was etched out using an etchant composed of 80% of phosphoric acid, 5% of acetic acid, 5% of nitric acid and 10% of deionized water. A mask was used to prevent etching the aluminum at the corner points for the samples in the first replicate and at two stripes in the middle for the samples in the second replicate. The unetched points or stripes were used to connect with the resistivity tool terminals. After etching process took place, the mask was removed by dissolving in acetone.

Resistivity measures were conducted using two techniques, van der Pauw and two stripes techniques. Van der Pauw was conducted on the first replicate, while the two stripes technique was conducted on the second replicate. In the van der Pauw technique, the voltage was