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Quality improvement of screen-printed Al emitter by using SiO_2 interfacial layer for industrial *n*-type silicon solar cells

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Abstract

This paper reports on an industrially applicable approach to create efficient Al-doped p^+ regions alloyed from screen-printed pastes for the application as rear emitters in *n*-type silicon solar cells. The influences of polished and pyramidal rear surfaces on the formation of Si–Al alloy and saturation current are discussed. We demonstrate that a thin SiO_2 layer on Si–Al interface can mitigate the inhomogeneous Al diffusion during alloying process and develop the transport properties. Furthermore, we apply this SiO_2 layer in our n^+np^+ solar cells, which exhibit lower series resistance and fine IQE response as a result of the improved Al emitter quality. For large-area *n*-type silicon solar cells (239 cm^2) with a full-area Al-p^+ rear emitter, we achieved an 18.8% efficient cell with an open-circuit voltage of 637.4 mV. Remarkable gains of 1.6% on average efficiency, 0.8 mA/cm^2 on J_{sc}, 8.6 mV on open-circuit voltage and 4.1% on FF are obtained, comparing with the solar cells fabricated by standard industrial process.

Keywords: *n*-type silicon solar cells; Screen-printing; SiO_2 layer; Aluminum-alloyed emitter

1. Introduction

N-type crystalline silicon wafer has attracted great attention of photovoltaic industries and scientific research, because it has higher tolerance against most of the common metal impurities (e.g. Fe) compared with p-type silicon (Macdonald and Geerligs, 2004), and it does not suffer from the boron-oxygen complexes related light-induced degradation (LID) Glunz et al. (2001). For laboratory solar cells with n^+np^+ or p^+nn^+structure, boron diffusion is mostly adopted to form p^+ emitter in order to obtain higher efficiency Bock et al. (2010), Benick et al. (2009), Untila et al. (2013). However, the boron diffusion is performed at 800–1000 °C, such high-temperature process induces crystallographic defects in the silicon bulks. Moreover, this energy consuming method is not suitable for industrial applications. Recently, alloying of screen-printed aluminum pastes has appeared as a technologically alternatives to boron diffusion. It allows a simplified p^+ emitter fabrication on *n*-type silicon wafers, and has become of growing interest in solar cell production Singh et al. (2011), Rauer et al. (2011), Moehlecke et al. (2013), Woehl et al. (2011) Book et al. (2011) Green (2003). The quality of Al-doped p^+ Si (Al-p^+) region is a crucial issue

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since it is related to the formation of p–n junction in n-type silicon solar cells. However, inhomogeneity of Al-doped p^+ Si layer is a common problem using the screen-printing method. Agglomerations and voids are frequently observed at the interface of Si–Al in industrial solar cells, which strongly affect the photovoltaic performances Huster (2005). Generally, the non-uniformity in emitter is believed to be caused by the contraction of Si–Al melt during alloying. The condition of back surface, the compositions of Al paste and the annealing processes are also relevant to the formation of p^+ Si layer. It is known that applying a thicker paste can mitigate the thickness inhomogeneity Rauer et al. (2011). Nevertheless, thicker paste usually aggravates the warp of wafers due to the contrast of thermal expansion coefficients between Si material and Al paste matrix. Therefore, it is quite important to investigate effective ways to realize high quality emitters for silicon solar cells.

In this study, we focus on the industrially feasible approaches to create efficient Al-doped emitters. We present a detailed characterization of full-area Al-p^+ regions, showing the influences of polished and pyramidal structures of rear surface on the saturation current density and the uniformity of Si–Al alloy. To obtain highly efficient solar cells, we propose to introduce a thin oxide layer at the interface of metal and silicon in our back junction structure. This layer can work as a buffer material on metal-silicon interface, mitigating the inhomogeneous Al diffusion during alloying process. Finally, we present new results for large-area (239 cm^2) industrial n-type Si solar cells featuring full-area and improved Al rear emitters.

2. Experimental methods

All experiments are carried out using (1 0 0)-oriented phosphorous-doped Czochralski (Cz) silicon wafers with a thickness of 200 μm and a resistivity of 1–3 Ω cm. For the J_{0e} measurements, we fabricate asymmetric test samples where the Al-p^+ emitter is on one side of the wafer, and the other surface of the sample is passivated with SiN_x. The test samples are sorted in two groups, by their pyramid textured and polished surfaces, as shown in Fig. 1(a) and (b). The random pyramidal surfaces are textured using alkaline and the polished surfaces are etched with a special solution. The Al-p^+ region is formed in an infrared conveyor belt furnace by firing the screen-printed Al pastes at 900 °C for 13 s. The residual Al paste and the Al–Si eutectic are finally removed in a boiling 37% solution of HCl. For the studies on solar cells, we fabricate cells in four groups featuring different rear surface conditions as shown in Fig. 2: group I cells are fabricated by standard industrial process with SiN_x front surface field (FSF) passivation and pyramid textured rear surface. In group II, the cells are with SiN_x FSF passivation and polished rear surface. Cells in group III are SiN_x/SiO_2 stack FSF passivated, rear surface polished and without rear interfacial oxide layer. Cells in group IV feature SiN_x/SiO_2 stack FSF passivation, polished rear surface and interfacial oxide layer. These cells are all of front contact back-junction structure, processed on 239 cm^2 wafers. After industrial texturing process and RCA cleaning, we perform an n^+ FSF phosphorus diffusion on the textured front surface, resulting in a FSF sheet resistance of 62 Ω/□. The phosphorus silicate glass (PSG) is subsequently etched off in HF solution. For cells with polished rear surface, we perform a single side wet chemical etch of about 3 μm. The oxide thin layers are grown from thermal oxidation at 850 °C on both sides of the samples. This SiO_2 layer is estimated to be 1.9 nm by ellipsometry measurement. For the cells in group III, HF solution is used to remove the oxidation layer on the rear side. To form the Al-p^+ rear emitter, industrial aluminum pastes are screen printed onto the rear surface and subsequently passed to alloying process. Prior to screen-printing the front contact grids, some samples are sorted out from group III and group IV for J_{0e} measurements, as shown in Fig. 1(c) and (d). All the other samples are then screen-printed with silver pastes on the SiN_x deposited front surfaces and finally fired in conveyor belt furnace.

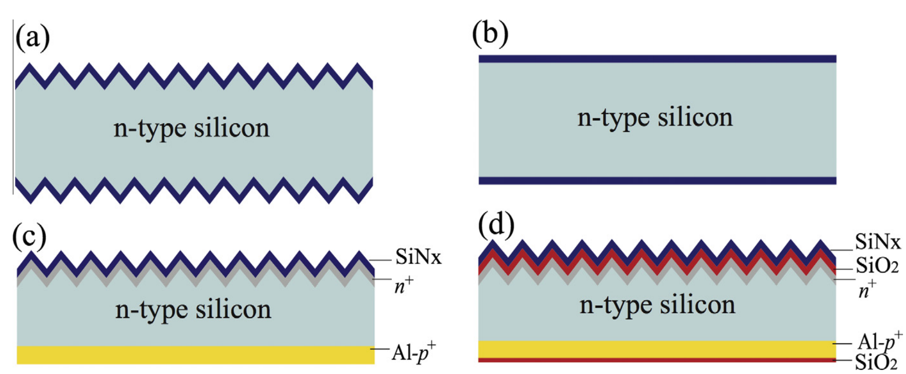

Fig. 1. Structures of the test samples used in this study for the characterization of J_{0e}. (a) A sample with double-sided pyramid textured surfaces and SiN_x passivation on both sides. (b) A sample with double-sided polished and SiN_x passivated surfaces. (c) A sample with pyramid textured front surface and polished rear surface. The front surface is n^+ diffused and SiN_x/SiO_2 stack passivated, the rear side is Al diffused. (d) A sample with pyramid textured front surface and polished rear surface. The front surface is n^+ diffused and SiN_x/SiO_2 stack passivated, and the rear side is Al diffused and SiO_2 coated.