



Enhanced absorption and short circuit current density of selective emitter solar cell using double textured structure

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Abstract

A double textured selective emitter (DTSE) solar cell was fabricated using Si wafer. The $40 \times 40 \text{ mm}^2$ silicon substrates were textured to form a pyramid-shaped surface, and nanowires were fabricated by a metal-assisted chemical etching process using Ag nanoparticles. All surface modifications of the micro and nanostructures were done by a wet-based process. The heavily doped and shallow emitters for selective emitter solar cells were prepared through the POCl_3 diffusion and a chemical etch-back process, respectively. The front and rear electrodes were prepared with a conventional screen printing method. The optical properties were enhanced through the double textured (DT) structure, and additional enhancement of the electrical properties was realized through the selective emitter concept. The DTSE solar cell achieved a higher conversion efficiency of 17.9% with improved absorption and short circuit current density compared to a DT solar cell.

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1. Introduction

Silicon (Si) is one of the most important materials in the photovoltaic (PV) industry because of its natural abundance and low toxicity. Thus, an opportunity for a low-cost manufacturing process is available (Conibeer et al., 2006; Green, 2003). Recently, the developments of many energy sources are in progress, and more innovations and technological advances are needed in the PV research area. Hence, maximizing the conversion efficiency of solar cells is

a key parameter while avoiding increased producing cost (Foldyna et al., 2013).

In order to enhance the conversion efficiency of the solar cell, there are two typical ways: optical and electrical enhancements. To improve the optical characteristics of solar cells, the modification of the surface morphology is one of the simple ways for more absorption of the incident light. Many approaches have been developed to enhance the optical aspects, such as texturing (Park et al., 2009) by using both wet and dry processes (Moreno et al., 2014), periodic gratings (Deceglie et al., 2012), nanostructures (Du et al., 2011; Han and Chen, 2010; Li et al., 2011) and luminescent downshifting (Griffini et al., 2015). In particular, Si nanowire arrays are good candidates for harvesting sunlight because of the light scattering effect. It has been reported that

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nanowire arrays realize low reflectance, and strong broadband optical absorption has been measured from the structure (Peng et al., 2005; Hu and Chen, 2007; Muskens et al., 2008). Based on these advantages, Si nanowires have been fabricated randomly or periodically through various methods such as the vapor–liquid–solid (VLS) method (Gunawan and Guha, 2009; Stelzner et al., 2008; Maiolo III et al., 2007), reactive ion etching (RIE) (Spurgeon et al., 2008), electrochemical etching, and metal-assisted chemical etching (Jaballah et al., 2012; Zhu et al., 2008; Sinakov et al., 2009; Garnett and Yang, 2008). Among these methods, metal-assisted chemical etching has attracted great attention because of its simple and low-cost process. Metal-assisted chemical etching methods enable Si nanowire arrays to be fabricated in a wet hood without expensive vacuum equipment. Another advantage is that there is no obvious size limitation (Huang et al., 2011).

One of the electrical modified models for the enhancement of conversion efficiency is the selective emitter solar cell (Lee et al., 2012). A highly doped emitter surface lowers the contact resistance with the front metal contact, while the lowly doped region, which is a shallow emitter, produces higher open circuit voltage (V_{OC}) and lowers losses of the converted charge carriers due to the reduced recombination in the emitter. Thus, combining these two concepts of metal-assisted chemical etching for optical aspects and a selective emitter for electrical aspects has a chance to improve the cell performance. In this paper, we fabricated Si nanowires on a pyramidal textured surface for double textured (DT) solar cells and double textured selective emitter (DTSE) solar cells. The specific flow for the fabrication of the solar cell is depicted in Fig. 1. Their optical and electrical properties, including the cell performance, were examined following the manufacturing process.

2. Experimental

2.1. Preparation for nanowires structure

The surface modification of pyramidal structures and Si nanowires was prepared through an all-wet-based process by texturing and electro-less etching using Ag nanoparticles. Chokralsky-grown 200- μm -thick p-type (100) solar-grade Si wafers ($\rho = 0.5\text{--}3.0 \Omega \text{ cm}$) were cut to the size of $40 \times 40 \text{ mm}^2$ for substrates. The nanowires structure was prepared by a texturing and electro-less etching process after the conventional texturing process. First, substrates were dipped into the NH_4OH and H_2O_2 solution with a mixing ratio of 4:1 at 80°C for 10 min to remove impurities. After the removal of native oxide layer on wafers by dipping in 1:10 diluted HF solution, substrates were dipped into a mixed solution consisting of 2 vol.% NaOH and 5 vol.% isopropyl alcohol with deionized water for 30 min. Then, textured wafers were immersed into a solution of 10 mM AgNO_3 and 4.8 M HF to precipitate Ag particles on the surface and etched for 45, 60, 75, and 90 s by dipping the wafers in an etching solution consisting of 4.8 M HF and 0.5 M H_2O_2 . Ag nanoparticles were removed after the etching process by dipping the samples in HNO_3 for 30 s.

2.2. Selective emitter solar cell process

A solar cell was fabricated through emitter doping by a phosphorous oxychloride (POCl_3) source using a diffusion furnace and conventional screen printing method. Samples were put into the diffusion furnace to form an n^{++} emitter layer using the POCl_3 source. Thermal diffusion was applied in ambient N_2 , O_2 , and POCl_3 gas at 860°C for 30 min. After the doping process, the phosphorus silica glass was removed by dipping in separate 1:10 diluted

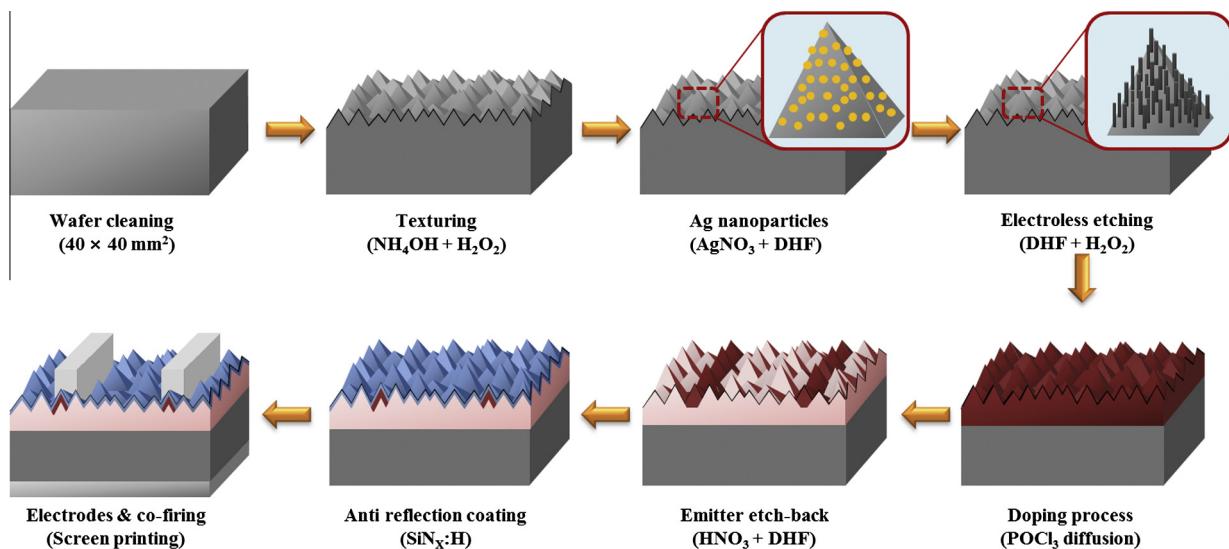


Fig. 1. The schematic diagram of process sequence for DTSE solar cell. Note that the schematic is not drawn to scale.

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