Accepted Manuscript

Performance analysis of gate all around GaAsP/AIGaSb CP-TFET

Alemienla Lemtur, Dheeraj Sharma, Priyanka Suman, Jyoti Patel, Dharmendra Singh Yadav, Neeraj Sharma

PII: S0749-6036(18)30538-X

DOI: 10.1016/j.spmi.2018.03.049

Reference: YSPMI 5579

To appear in: Superlattices and Microstructures

Received Date: 17 March 2018

Accepted Date: 19 March 2018

Please cite this article as: A. Lemtur, D. Sharma, P. Suman, J. Patel, D.S. Yadav, N. Sharma, Performance analysis of gate all around GaAsP/AlGaSb CP-TFET, *Superlattices and Microstructures* (2018), doi: 10.1016/j.spmi.2018.03.049.

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.



Performance Analysis of gate all around GaAsP/AlGaSb CP-TFET

Alemienla Lemtur, Dheeraj Sharma, Priyanka Suman, Jyoti Patel, Dharmendra Singh Yadav, Neeraj Sharma

Electronics and Communication Engineering Discipline, PDPM-Indian Institute of Information Technology, Design and Manufacturing Jabalpur 482005, M.P and Department of Computer Science Engineering Ramrao Adik Institute of Technology Nerul, Navi Mumbai,400706, INDIA.

Abstract

Illustration of importance of gate all around (GAA) structure and heterojunction formed by III-V semiconductor compounds has been analysed through GaAsP/AlGaSb CP-TFET (charge plasma tunnel field effect transistor). Charge plasma concept has been incorporated here to make this device more immune towards random dopant fluctuations (RDF). A high driving current of 1.28×10^{-5} A/ μ m and transconductance (g_m) of 96.4 μ S at supply voltages V_{GS}= 1V and V_{DS}= 0.5V is achieved. Further, implications of employing this device in analog/RF circuits have been supported with simulated results showing a high cut-off frequency of 34.5 THz and device efficiency of 3.45 MV⁻¹. Apart from this, an insight of the linearity performances has also been included. Simultaneously, all the results are compared with a conventional gate all around charge plasma TFET.

Keywords: GAA, charge plasma, RDF, hetero-junction.

Email addresses: alemlmtr780gmail.com (Alemienla Lemtur),

dheeraj24482@gmail.com (Dheeraj Sharma), priyankasuman007@gmail.com (Priyanka Suman), ivotipatelac39@gmail.com (Ivoti Patel)

(Priyanka Suman), jyotipatelec39@gmail.com (Jyoti Patel),

tech.dharmendra26@gmail.com (Dharmendra Singh Yadav), neeraj16ks@gmail.com (Neeraj Sharma)

Download English Version:

https://daneshyari.com/en/article/7938934

Download Persian Version:

https://daneshyari.com/article/7938934

Daneshyari.com