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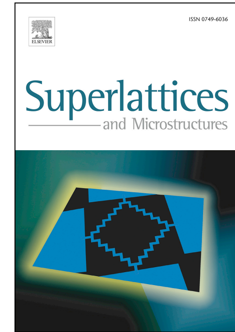

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ACCEPTED MANUSCRIPT

Modeling the instability behavior of thin film devices: Fermi Level Pinning

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Abstract

We investigate the underlying physics of degradation/recovery of a metal/n-CdTe Schottcky junction under reverse or forward bias stressing conditions. We used Sah-Noyce-Shockley (SNS) theory to investigate if the swept of Fermi level pinning at different levels (under forward/reverse bias) is the origin of change in current-voltage characteristics of the device. This theory is based on Shockley-Read-Hall recombination within the depletion width and takes into account the interface defect levels. Fermi Level Pinning theory was primarily introduced by Ponpon and developed to thin film solar cells by Dharmadasa's group in Sheffield University-UK. The theory suggests that Fermi level pinning at multiple levels occurs due to high concentration of electron-traps or acceptor-like defects at the interface of a Schottky or pn junction and this re-arranges the recombination rate and charage collection. Shift of these levels under stress conditions determines the change in current-voltage characteristics of the cell. This theory was suggested for several device such as metal/n-CdTe, CdS/CdTe, CIGS/CdS or even GaAs solar cells without a modeling approach to clearly explain it's physics. We have applied the strong SNS modeling approach to shed light on Fermi Level Pinning theory. The modeling confirms that change in position of Fermi Level and it's pining in a lower level close to Valence band increases the recombination and reduces the open-circuit voltage. In contrast, Fermi Level pinning close to conduction band strengthens the electric field at the junction which amplifies the carrier collection and boosts the open-circuit voltage. This theory can well explain the stress effect on device characteristics of various solar cells or Schottky junctions by simply finding the right Fermi level pinning position at every specific stress condition.

Keywords: Modeling, Degradation, Recovery, Fermi Level Pinning, Thin Film, CdTe.

1. Introduction

In 1985, the concept of Fermi Level Pinning (FLP) was proposed for the first time to explain the current-voltage characteristics of CdTe based Schottky barriers [1]. In 2005, Dhramadasa et al developed this concept to explain the variation observed in the current-voltage (JV) characteristics of metal/n-CdTe single devices [2]. They proposed that any change in JV curves (degradation/recovery) at normal operation condition or under stress condition might be due to change in position of the Fermi level (E_f). The Fermi level will be pinned at one of the 5 defective levels at the interfaces due to high concentration of trap density at the junction. For example, at CIGS/metal interface, 4 different Fermi pinning levels were measured: 0.77, 0.84, 0.93, 10.3 ±0.02 eV [6, 7]. These multiple levels arise form the high concentration of defects at the interface of the device during the fabrication process and change from one device to another. This concept was also extended to explain the instability behavior of CdTe and $Cu(In,Ga)(Se,S)_2$ based thin film solar cells [3, 4]. The FLP theory explains: under forward bias all the 5 defective levels will be below the Fermi level and, therefore, the defects will trap the electrons reducing the open-circuit voltage of the cell (V_{oc}). In contrast, under the reverse-bias sweep, all the defect levels are above the Fermi level and, therefore, the defects will de-trap electrons during this period. This also can occur under stress conditions which could alter the leveling between the E_f and multiple pinning levels or trap levels and the band alignment at the interface where the electric field collects the generated carriers. Stress condition is well effective on FLP: Fermi level pinning position moves upward under prolonged irradiation which can significantly increase the carrier trapping resulting a lower open-circuit voltage, V_{oc}.Prolonged irradiation is equivalent to forward biasing where the dark rest conditions is equivalent to zero biasing of the cell. Therefore, these stressing or recovery conditions during daytime and night-time can be explained in terms of trapping and de-trapping of electrons by slow defects at pinning levels. This concept can thus explain the carrier transport and the observed changes in current-voltage characteristics or the degradation/recovery of device metrics under stress conditions. We have already considered different approaches to explain the device degradation under illumination, temperature, and long term biasing of thin films [5] and in this paper we will further focus on Fermi level pinning as a simple and practical approach.

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