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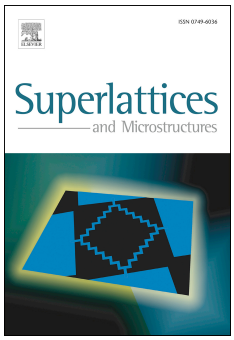

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Impact of scaling voltage and size on the performance of Side-contacted Field Effect Diode

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Abstract

Side-contacted Fild Effect Diode (S-FED), with low leakage current and high I_{on}/I_{off} ratio, has been recently introduced to suppress short channel effects in nanoscale regime. The voltage and size scalability of S-FEDs and effects on the power consumption, propagation delay time, and power delay product have been studied in this article. The most attractive properties are related to channel length to channel thickness ratio in the S-FED which reduces in comparison with MOSFET significantly, while gates control over the channel improve and the off-state current reduces dramatically. This promising advantage is not only capable to improve important S-FED's characteristics such as subthreshold slope but also eliminate Latch-up and floating body effect.

Keywords: logic gates, nanoscale devices, scalability, side-contacted FED.

1. Introduction

Scalability is extremely important issue in digital designing whether about scaling channel length or voltage. Operation of digital blocks can be optimized in term of voltage and frequency as if it works properly with maximum performance without overheating so dynamic voltage/frequency scaling (DVFS) were proposed to choose minimum supply voltage for optimizing clock frequency and power consumption [1,2].

Field Effect Diode (FED) has been proposed not only for increasing drive current but also operating in different application such as dynamic memory cell (DRAM), static memory cell (SRAM), electrostatic discharge (ESD), high speed digital circuit [3-7]. In very short channel length below 100 nm, FED faces with multiple challenges such as large off-state current. To supress such defects, S-FED was introduced and optimised geometrically [8,9]. Recently demonstrated that S-FED can be a part of logic circuit both in high frequency and low power designing [10,11].

Comparable study between SOI-MOSFET and S-FED led to distinguish superior advantages in term of subthreshold slope (SS), threshold voltage (V_{th}) and on state to off state current ratio (I_{on}/I_{off}). Also Mixed-mode simulation assisted to realize S-FED's operation into the inverter logic gate in comparison with CMOS counterpart. To have a fairly comparison, all parameters for both S-FED and MOSFET were considered exactly the same: 10^{+21} cm^{-3} source and drain doping concentrations, 25, 45, 55 and 95 nm channel length, 0.8 nm gate oxide, 145 nm buried oxide (BOX) thickness and gate work function of 4.7 eV. Equivalent