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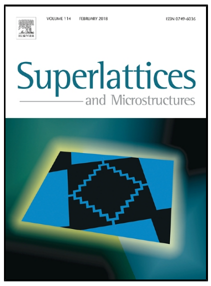

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Control of short-channel effects in InAlN/GaN high-electron mobility transistors using graded AlGaN buffer

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Abstract: A graded AlGaN buffer is designed to realize the p-type buffer by inducing polarization-doping holes. Based on the two-dimensional device simulator, the effect of the graded AlGaN buffer on the direct-current (DC) and radio-frequency (RF) performance of short-gate InAlN/GaN high-electron mobility transistors (HEMTs) are investigated, theoretically. Compared to standard HEMT, an enhancement of electron confinement and a good control of short-channel effect (SCEs) are demonstrated in the graded AlGaN buffer HEMT. Accordingly, the pinched-off behavior and the ability of gate modulation are significantly improved. And, no serious SCEs are observed in the graded AlGaN buffer HEMT with an aspect ratio (L_G/t_{ch}) of about 6.7, much lower than that of the standard HEMT (L_G/t_{ch} =13). In addition, for a 70-nm gate length, a peak current gain cutoff frequency (f_T) of 171 GHz and power gain cutoff frequency (f_{max}) of 191 GHz are obtained in the grade buffer HEMT, which are higher than those of the standard one with the same gate length.

Keyword: InAlN/GaN, Graded AlGaN, HEMT, Back barrier, Short-channel effects

1. Introduction

The lattice-matched $In_{0.17}Al_{0.83}N$/GaN high-electron mobility transistors (HEMTs), with the strong spontaneous polarization and strain-free barrier, are emerging as the promising candidate for high-frequency and high-power applications [1-5]. To operate the devices in millimeter frequency, it is necessary to shorten the gate length (L_G). However, as the gate length scaling down, a sufficiently high aspect ratio (L_G/t_{ch}, where t_{ch} is the gate-to-channel separation) cannot always be maintained for an adequate gate control to channel [6]. Especially, for the ultrashort-gate devices, short-channel effects (SCEs), such as threshold-voltage shift, high sub-threshold swing and increased drain conductance, seriously hinder the improvement of the device performance. Uren et al. [7] reports that SCEs mainly originate from the poor electron confinement at the channel bottom. At high drain-source voltages, even if the gate bias is high enough to pinch off the channel, the current leakage path can be formed within the deep of the buffer. Therefore, in an insufficient aspect ratio case, the buffer design is an important alternative solution to control SCEs.

To increase the resistivity of the GaN buffer, an effective way is to dope iron (Fe) or carbon (C) acceptors for compensating the bulk free electrons in the buffer [8]. However, this would enhance the electron trapping in the buffer and therefore the current collapse [9]. Another buffer design is back-barrier technology [10-13], which

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