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A dual channel three-terminal np-LDMOS with both majorities for conduction

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ABSTRACT

A novel dual channel three-terminal np-LDMOS power device with both electrons and holes for conduction is proposed in this paper. Based on a new approach of inducing a large-signal which is processed by a simple circuit for controlling the gate of p-LDMOS inside the device, the new np-LDMOS only requires one external gate controlling voltage signal that can be performed as an n-LDMOS device. The SOA of the new device is improved in comparison with the n-LDMOS device, since the counteracting of electric flux density produced by the both type of carriers' currents. Furthermore, the specific on-resistance of the np-LDMOS device is reduced by about 19% when comparing with that of the conventional one. The control method and performances of the proposed power device are investigated and authenticated by numerical simulations.

1. Introduction

The lateral double-diffused metal-oxide semiconductor (LDMOS) devices are crucial components in many power amplifiers and intelligent power applications with its compatible manufacturing process [1,2]. However, at present the contradiction between higher breakdown voltage (*BV*) and lower specific on-resistance (R_{SP}) is still existent in LDMOS devices, although some measures, such as REduced SURface Field (RESURF) [3–7] and OPTimum Variable Lateral Doping (OPTVLD) are employed [8–11]. The OPTVLD technique is regarded as an excellent trade-off performance between the *BV* and R_{SP} of unipolar LDMOS devices. But, it is always expected that the R_{SP} is to be infinitely low for any given *BV* of the devices. Moreover, there is a "sharp rise" in the current-voltage characteristics (I–V curves) when an unipolar LDMOS device operates on the status of a high voltage and a large current, which results in a significant reducing of the reliability and safe operating area (SOA) [12,13].

In order to alleviate the problems stated above, a new LDMOS device with the idea of employing majority carriers of both electrons and holes for conduction was proposed [12]. The device (known as np-LDMOS) is a double-gate structure which a high voltage OPTVLD n-LDMOS device is integrated with a high voltage PMOS device by using the same drift region. Thus, the holes of the PMOS can counteract the effect induced by the electrons of the n-LDMOS on the drift region when the device is working on the condition of a high voltage and a large current. After that, some feasible approaches have been proposed to develop the four-terminal device to be a three-terminal one [13,14]. However, there are some drawbacks in these approaches: the self-generated gate controlling signal of PMOS is very weak resulting in a high probability of noise distribution and a very

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complicated low voltage signal processing circuit [13], or the PMOS is only turned on when the device is working on the state of the drain to source voltage more than 9 V ($V_{DS} > 9$ V), which cannot lead to a lower R_{SP} [14]. At the same time, like other dual-channel LDMOS structures presented in Refs. [15–18], the devices are all four-terminal ones, which bring new challenges to application and cannot be used for substituting the conventional three-terminal n-LDMOS or p-LDMOS power devices directly.

In order to achieve a dual channel three-terminal np-LDMOS device with an ultralow R_{SP} and a better SOA, a novel internal signal generating approach and a very simple low voltage CMOS signal processing circuit for controlling the gate of PMOS are proposed in this paper. And the specifics are depicted in the subsequent sections.

2. Device structure and controlling method

The structure of the proposed np-LDMOS device is based on OPTVLD technique [12–14], which is shown in Fig. 1(a) (The electrodes or connection nodes with the same name are connected together inside the chip in Fig. 1). The p-top region, n-well region and p-bury region constitute an OPTVLD voltage-sustaining region (or drift region). The n-LDMOS M_N consists of source (*S*), gate (*G*), n-well region and drain (*D*); and the high voltage PMOS M_P is composed of the drain (*D*), gate (G_P), p-top region and the source (*S*). It is apparent that both the n-LDMOS M_N and the PMOS M_P share the same voltage sustaining region, so they have the same *BV*. The two dashed lines of the structure are the depletion boundaries when the drain to source voltage V_{DS} is applied with the breakdown voltage (650 V in this paper) of the device. Meantime, it is easy to see that the left side and the right side of the structure are almost symmetrical, and the only difference between the two sides is the connections of electrodes *F* and *H* inside the chip. The electrode *F* is utilized to generate a pulse voltage signal referred to electrode *D* (the generated pulse voltage signal $V_{FD} = V_F - V_D$) while M_N is switching under the controlling of its gate pulse voltage signal V_{GS}. The electrode *H* is connected in series with diode D_0, electrode *E*, capacitor *C* and electrode *D* to compose a negative low voltage power source V_{ED} ($V_{ED} = V_E - V_D$, the potential difference between electrodes *E* and *D*), which is used for providing energy for the low voltage circuit (LVC) shown in Fig. 1.

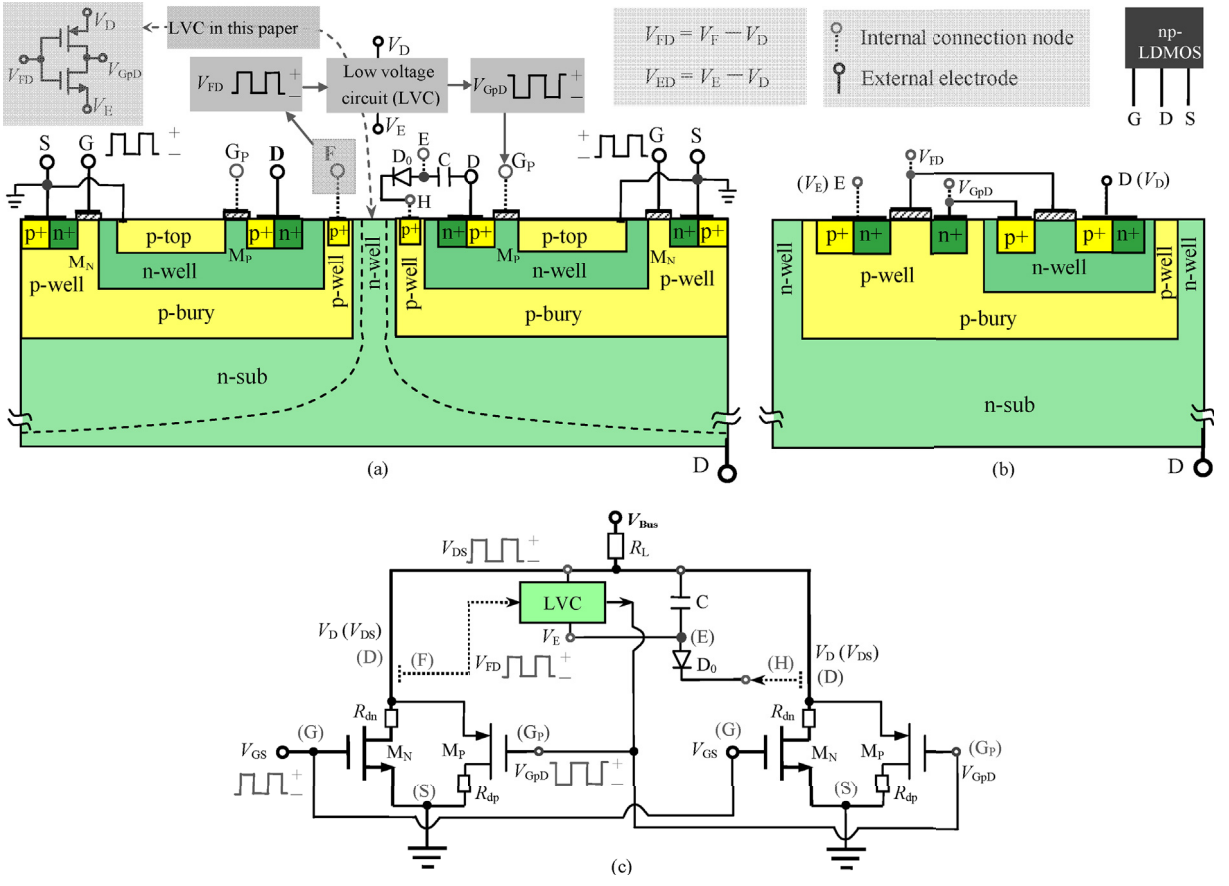

Fig. 1. (a) The structure and controlling process of the proposed np-LDMOS, (b) structure of the low voltage circuit (LVC) made in the middle neutral n-well region shown in (a) and (c) the equivalent circuit of the proposed structure. (The electrodes or connection nodes with the same name are connected together inside the chip.)

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