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The GaN trench gate MOSFET with floating islands: High breakdown voltage and improved BFOM

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ABSTRACT

A novel GaN trench gate (TG) MOSFET with P-type floating islands (FLI) in drift region, which can suppress the electric field peak at bottom of gate trench during the blocking state and prevent premature breakdown in gate oxide, is proposed and investigated by TCAD simulations. The influence of thickness, position, doping concentration and length of the FLI on breakdown voltage (BV) and specific on-resistance (R_{on_sp}) is studied, providing useful guidelines for design of this new type of device. Using optimized parameters for the FLI, GaN FLI TG-MOSFET obtains a BV as high as 2464 V with a R_{on_sp} of 3.0 mΩ cm^2. Compared to the conventional GaN TG-MOSFET with the same structure parameters, the Baliga figure of merit (BFOM) is enhanced by 150%, getting closer to theoretical limit for GaN devices.

1. Introduction

GaN, as a member of 3rd generation semiconductors, has a significant potential in high power and high speed applications due to its wide energy band gap of 3.4eV, high critical breakdown field of 3.3 MV/cm and high saturation velocity of 2.5×10^7 cm/s [1,2]. Recently, GaN-based power devices, especially high electron mobility transistors (HEMTs) on silicon substrate, are widely explored and trigger commercial interest because of their relatively simple manufacturing process and low-cost substrate [3–6]. However, the heteroepitaxy GaN on silicon suffers from challenges in improving the performance and reliability of AlGaN/GaN HEMTs, like current collapse and premature breakdown. A vertical MOSFET structure is widely adapted for Si-based power devices, enabling a higher current density within a small chip area and reducing parasitic effects [7,8]. Despite the relatively complicated fabrication process, vertical GaN power devices make it easier to realize enhancement mode operation and avalanche breakdown to achieve the best figure of merit (FOM) [9,10]. A GaN-based trench gate MOSFET (TG-MOSFET), recently reported by TOYODA GOSEI has set a record for normally-off GaN power devices [11,12]. However, the reported values are still far away from the theoretical limit for GaN devices because of premature breakdown in the gate dielectric at the trench corners, which is a symptomatic problem for TG-MOSFETs. Thus, it is of great importance to optimize the GaN TG-MOSFET design to prevent the electric field crowding at the trench corners. As reported in Refs. [13,14], the floating island (FLI) concept was proposed for silicon TG-MOSFETs in order to break the theoretical silicon limit for Si-based

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power devices by reducing the peak field in the drift region and realizing a lower specific on-resistance. This idea has also been applied to SiC TG-MOSFETs, achieving the same effect of suppressing the high electric field in the gate oxide and thus enhancing the breakdown voltage [15,16]. However, the effect of FLI for GaN TG-MOSFETs has not been investigated yet and the role of various device parameters for GaN TG-MOSFETs with FLI to guide the device optimization has not been reported. Additionally, the FLI concept is relatively easy to realize in case of GaN by a multiple epitaxial overgrowth process compared to a more complex superjunction technology, Because superjunction should be made by several times of alternate epitaxial overgrowth and ion implantation process, and good charge balance between P and N columns cannot be maintained even if fabricatable [17].

A novel GaN TG-MOSFET with FLI (FLI TG-MOSFET) is proposed in this paper and the main focus is to examine effect of the FLI by two-dimensional (2D) device simulations using the Sentaurus Device Simulator that how the existence of FLI contributes to shield the gate oxide at the bottom of the gate trench from the high electric field during the blocking state, meanwhile improving the Baliga's figure of merit (BFOM). Moreover, the effect of doping concentration, length and position of the FLI on breakdown voltage (BV) and specific on-resistance (R_{on_sp}) is investigated, and an optimized structure is put forward. Regarding to BFOM, the FLI TG-MOSFET shows better performance than the best reported results for normally-off GaN-based power devices, closer to theoretical limit for GaN.

2. Device structure and models

Firstly, the reported experimental results of a conventional GaN TG-MOSFET in Ref. [11] have been investigated As a benchmark test for our simulations. Fig. 1(a) illustrates the structure of the conventional GaN TG-MOSFET. The structure parameters used in the simulation are based on the reported values, as indicated in Table 1. In the following, we briefly summarize relevant models used in simulations. The mobility models include concentration dependent mobility with high field saturation effect. The effect of mobility degradation due to interface charge scattering is considered by the model of “enormal”. Additionally, the Schockley-Read-Hall (SRH) recombination model and the impact ionization model of Okuto Crowell are utilized. Avalanche breakdown in the GaN is determined to occur when the ionization rate integral value all over the device reaches one, and the breakdown of the gate dielectric is defined to occur once the maximum electric field in gate oxide is beyond the critical electric field (10 MV/cm) of SiO_2 deposited by ALD [18]. As shown in Fig. 1(e), the simulated transfer characteristics of the conventional GaN TG-MOSFET are in good agreement with the experiment results when the constant electron mobility is fitted to be 300 cm^2/V and the fixed charge concentration is set as 2.5×10^{12} cm^{-2} and 1.3×10^{18} cm^{-3} at GaN/oxide interface and in oxide gate dielectric, respectively. It validates the correctness of simulation models and parameters. Thus the extracted values for the electron mobility and fixed charge concentration are used in the following simulation of GaN FLI TG-MOSFET. For the blocking characteristics, the simulated breakdown voltage (BV) is 1200 V with a trench depth (tr) of 0.3 μm, which is the same as reported value of the benchmark. Fig. 1(c) shows the 2D electric field distribution across the benchmark device at the breakdown point (1200 V) and the electric field peak is found to occur around the trench corners (X = 5.3 μm and 7.3 μm) in GaN ($E_{PTC\text{-}GaN}$) and SiO_2 ($E_{P\text{-}SiO2}$). $E_{P\text{-}SiO2}$ reaches the critical breakdown value of SiO_2. The electric field distribution along the y-axis at X = 5.3 μm is extracted and shown in Fig. 1(f). The peak electric field in GaN is far away from the critical breakdown value, thus indicating that breakdown occurs in gate oxide rather than avalanche in GaN (see Table 2).

In the FLI TG-MOSFET (Fig. 1(b)), a P-type layer is inserted to the drift region so that the drift layer is formed by two regions. Under reverse bias condition, another electric field peak is induced by the insertion of FLI. Thus, theoretically, it is easier for GaN FLI TG-MOSFET to obtain a higher BV than conventional GaN TG-MOSFET, even with the same N-drift doping concentration. For comparison, the electric field distribution at a drain voltage of 1200 V for the GaN FLI TG-MOSFET with the same structure parameters is simulated and shown in Fig. 1(d). Apart from the electric field peak at the trench corner, the existence of FLI induces another electric field peak at the lower interface of the FLI and drift region ($E_{P\text{-}FLI}$). The two electric field peaks are investigated by analysing the electric field distribution along y-axis at X = 1.2 μm and 5.3 μm and shown in Fig. 1(f). Compared with conventional structure, the value of the electric field peak at the trench corners in GaN and gate oxide is effectively suppressed by the FLI at the same drain bias. Therefore the premature breakdown phenomenon in the gate oxide is suppressed and BV of the device is improved.

3. Results and discussions

In order to understand the influence of FLI geometry parameters on device performance, simulations with various thickness (t_p), distance to P-Well (D_p), length (L_p) and doping concentration (N_p) (Fig. 1(b)) have been performed.

3.1. Effects of thickness of the FLI on blocking characteristics

Fig. 2(a) shows BV of a GaN FLI TG-MOSFET with different FLI position (D_p) against FLI thickness (t_p). L_p and N_p are set as 4 μm and 1×10^{17} cm^{-3} in the simulations. BV of the device versus t_p shows a peak value for each investigated position D_p and reaches a maximum value at $D_p = 4.3$ μm. The electric field distribution along the y-axis at X = 5.3 μm and X = 1.2 μm for different t_p at $D_p = 4.3$ μm is shown in Fig. 2(b). The electric field peak $E_{PTC\text{-}GaN}$ decreases with increasing t_p, accompanied with the decrease of $E_{P\text{-}SiO2}$, thus breakdown mechanism of the device changes from premature breakdown in the gate

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