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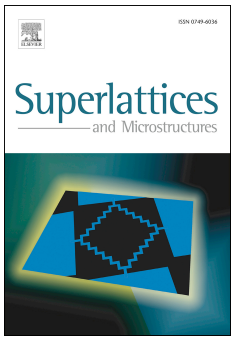

Analytical model of nanoscale junctionless transistors towards controlling of short channel effects through source/drain underlap and channel thickness engineering

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Analytical model of nanoscale junctionless transistors towards controlling of short channel effects through source/drain underlap and channel thickness engineering

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Abstract **-We develop a 2D analytical subthreshold model for nanoscale double-gate junctionless transistors (DGJLTs) with gate-source/drain underlap. The model is validated using well-calibrated TCAD simulation deck obtained by comparing experimental data in the literature. To analyze and control short-channel effects, we calculate the threshold voltage, drain induced barrier lowering (*DIBL*) and subthreshold swing of DGJLTs using our model and compare them with corresponding simulation value at channel length of 20nm with channel thickness t_{Si} ranging 5–10nm, gate-source/drain underlap (L_{SD}) values 0–7nm and source/drain doping concentrations (N_{SD}) ranging 5-12×10^{18} cm^{-3}. As t_{Si} reduces from 10 to 5nm *DIBL* drops down from 42.5 to 0.42mV/V at N_{SD}=10^{19} cm^{-3} and L_{SD}=5 nm in contrast to decrement from 71 to 4.57mV/V without underlap. For a lower t_{Si} *DIBL* increases marginally with increasing N_{SD}. The subthreshold swing reduces more rapidly with thinning of channel thickness rather than increasing L_{SD} or decreasing N_{SD}.**

Keywords: **Junctionless transistor, gate-source/drain underlap, model, short channel effects, TCAD**

1. Introduction

Of late junctionless transistors (JLTs) have shown promise for both analog/RF and logic circuit applications owing largely to their excellent turn-on and subthreshold characteristics endowed with a low OFF-current [1-6]. In contrast to inversion mode (IM) transistors in which extraordinarily high doping concentration gradient needs to be maintained between source/channel and drain/channel junctions, JLTs having no semiconductor-semiconductor junctions feature easy scalability to 20 nm and beyond thereby making them particularly suitable for digital circuit applications. In addition, JLTs exhibit better immunity to short channel effects (SCEs) due to absence of source-channel and drain-channel junctions and thus eliminating the possibility of any charge sharing between them.

There have been several recent studies reported in the literature [7-18] on the modeling and simulation of junctionless transistors. Hu et al. [14] developed an analytical model for surrounding gate JL transistors with no source/drain underlap assuming full depletion in the channel. A compact drain current model for long channel gate