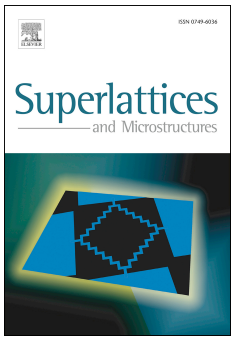
Accepted Manuscript



Performance improvement of doped TFET by using plasma formation concept

Deepak Soni, Dheeraj Sharm, Shivendra Yadav, Mohd. Aslam, Neeraj Sharma

PII: S0749-6036(17)31576-8

DOI: 10.1016/j.spmi.2017.10.012

Reference: YSPMI 5306

To appear in: *Superlattices and Microstructures*

Received Date: 29 June 2017

Revised Date: 10 October 2017

Accepted Date: 12 October 2017

Please cite this article as: D. Soni, D. Sharm, S. Yadav, M. Aslam, N. Sharma, Performance improvement of doped TFET by using plasma formation concept, *Superlattices and Microstructures* (2017), doi: 10.1016/j.spmi.2017.10.012.

Performance Improvement of Doped TFET by Using Plasma Formation Concept

Deepak Soni, Dheeraj Sharma, Shivendra Yadav, Mohd. Aslam, *Neeraj Sharma

Nanoelectronics and VLSI Lab.
Electronics and Communication Engineering Discipline
PDPM Indian Institute of Information Technology, Jabalpur, 482005, India.
Department of Computer Engineering,*
Ramrao Adik Institute of Technology Nerul, Navi Mumbai India*

Abstract

Formation of abrupt doping profile at tunneling junction for the nanoscale tunnel field effect transistor (TFET) is a critical issue for attaining improved electrical behaviour. The realization of abrupt doping profile is more difficult in the case of physically doped TFETs due to material solubility limit. In this concern, we propose a novel design of TFET. For this, P^+ (source)-I (channel)-N (drain) type structure has been considered, wherein a metal electrode is deposited over the source region. In addition to this, a negative voltage is applied to the source electrode (SE). It induces the surface plasma layer of holes in the source region, which is responsible for steepness in the bands at source/channel junction and provides the advantage of higher doping in source region without any addition of the physical impurity. The proposed modification is helpful for achieving steeper band bending at the source/channel interface, which enables higher tunneling generation rate of charge carriers at this interface and overcomes the issue of low ON-state current. Thus, the proposed device shows the increment of 2 decades in drain current and 252 mV reduction in threshold voltage compared with conventional device. The optimisation of spacer length (L_{SG}) between source/gate

Email addresses: deepaksoni09@gmail.com (Deepak Soni), dheeraj24482@gmail.com (Dheeraj Sharma), shivendra1307@gmail.com (Shivendra Yadav), mohd.aslam22d@gmail.com (Mohd. Aslam), neeraj16ks@gmail.com (*Neeraj Sharma)