Superlattices and Microstructures xxx (2017) 1–9

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Suppression of threshold voltage variability in MOSFETs by adjustment of ion implantation parameters

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ARTICLE INFO

Article history:
Received 19 September 2017
Received in revised form 30 October 2017
Accepted 30 October 2017
Available online xxx

Keywords:
Random dopant fluctuation
Impedance field method
Threshold voltage variability
Sense amplifier
Ion implantation
MOSFET

ABSTRACT

In this study, we investigate threshold voltage (V_{TH}) variability of metal-oxide-semiconductor field-effect transistors induced by random dopant fluctuation (RDF). Our simulation work demonstrates not only the influence of the implantation parameters such as its dose, tilt angle, energy, and rotation angle on the RDF-induced V_{TH} variability, but also the solution to reduce the effect of this variability. By adjusting the ion implantation parameters, the 3σ (V_{TH}) is reduced from 43.8 mV to 28.9 mV. This 34% reduction is significant, considering that our technique is very cost effective and facilitates easy fabrication, increasing availability.

1. Introduction

In nanoscale complementary metal-oxide-semiconductor (CMOS) technology, process-induced threshold voltage (V_{TH}) variations between identically designed metal-oxide-semiconductor field effect transistors (MOSFETs) are major issues [1]. Threshold voltage differences between MOSFETs consisting of sense amplifiers in the dynamic random access memory (DRAM) induce increasing errors in reading memories in digital CMOS circuits [2]. Process-induced V_{TH} variations originate from random dopant fluctuation (RDF), line-edge roughness, and work-function variation. Among these variation sources, RDF is regarded as the dominant factor affecting the threshold voltage variation in MOSFETs [3]. RDF results from the variation in concentration and position of dopants in their channels [4]. During the ion implantation and diffusion process, unintended dopants penetrate the channels, causing threshold voltage variations due to their random distribution [5]. In order to reduce the threshold voltage variation, research groups have suggested some methods, including forming steep retrograde channel profiles [6], reducing the gate dielectric thickness [7], and developing new device architectures [8]. However, less attention has been paid to reducing the threshold voltage variation without changing the physical dimensions. In this study, we propose a route to reduce threshold voltage variation in MOSFETs by adjusting ion implantation parameters, such as their dose, tilt angle, energy, and rotation angle, to control the vertical doping profiles of their channels. The variation in the performance of MOSFETs is one of the major obstacles for future process generation [9], and thus reducing the threshold voltage variation by adjusting its parameters definitely benefits the semiconductor industry in terms of cost and ease of fabrication.

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https://doi.org/10.1016/j.spmi.2017.10.034
0749-6036/

2. Device structure and simulation methodology

Fig. 1(a) shows a schematic design of an n-channel MOSFET (n-MOSFET) in the three-dimensional view, and Fig. 1(b) presents the cross-section (A-A′). The device simulation was established with the dimensional parameters, including a gate length of 120 nm, a gate width of 500 nm, and a gate oxide thickness of 2 nm. As shown in Fig. 1(a) and (b), the gate channel and the gate oxide materials are silicon and SiO_2, respectively. Furthermore, polysilicon heavily doped with phosphorus ions served as the gate electrode. Our simulation work was carried out with a three-dimensional structure, following a process flow illustrated in Fig. 1(c). In order to realize an n-MOSFET in our simulation work, the source and the drain regions were formed by doping high concentrations of arsenic and phosphorus ions in the *p*-type silicon bulk through the lightly doped drain (LDD) and the source/drain (S/D) implantations. In addition, halo implantation was performed by implanting boron ions with a tilt angle of 45°, an energy of 10 keV, and a rotation angle of 45° to lessen the short channel effect. In addition, the carbon implantation was applied before the halo, LDD, and S/D implantations to mitigate the transient enhanced diffusion that aggravates the random dopant fluctuation in the device [10]. In our simulated device, the shadowing effect does not need to be considered, because the ion implantation is applied to a half of the device structure, and the rest half of the structure is reflected to form the full transistor at the end of the process.

For the analysis, the device simulation was performed using the Synopsys Sentaurus Device (version L-2016.03) [11] with a drift-diffusion transport model for calculating current densities of electrons and holes, the old Slotboom model for band gap narrowing, and the Shockley-Read-Hall recombination model. Furthermore, three mobility models were adopted; the Philips unified mobility model for majority and minority carrier mobility, the high field saturation model for velocity saturation, and the transverse field dependence model for mobility degradation at the interfaces. In addition, the noise model for investigating the random dopant fluctuation was adopted in order to activate the fluctuations in the doping concentration.

V_{TH} variability induced by RDF in n-MOSFET was investigated through the impedance field method (IFM) approach. IFM, a simulation method based on the linear response theory, computes fluctuations in the device using Green's functions for statistical variability analysis [12]. Details on the advantages of IFM are available in the Supplementary materials.

3. Results and discussion

3.1. Characterization of V_{TH} variability induced by RDF

The simulated drain-to-source current *versus* the gain-to-source voltage (I_{DS}–V_{GS}) transfer curves for an n-MOSFET with random doping profiles are shown in Fig. 2(a). The samples utilized for RDF was 1,000, and these samples were generated through the IFM approach. Furthermore, for reference, the curve for the reference device with a continuum doping profile is

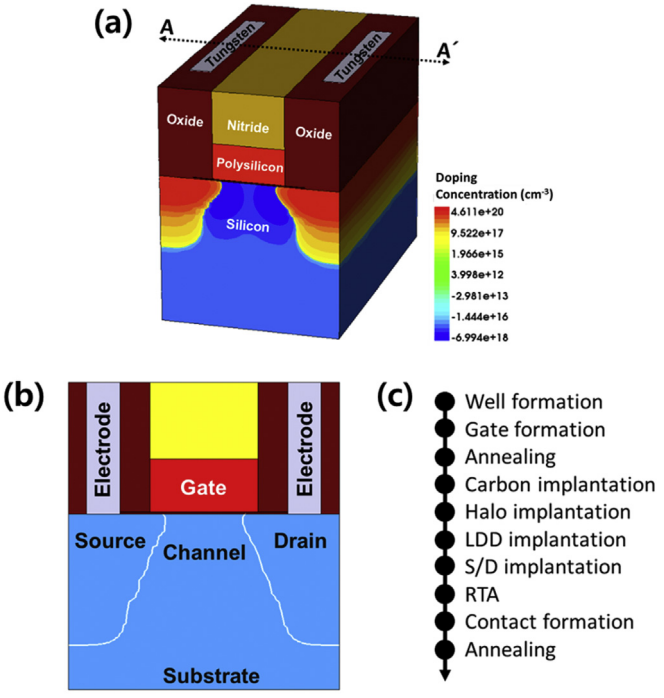

Fig. 1. (a) Three dimensional image, (b) schematic cross-section, and (c) process flow chart of n-MOSFET for TCAD simulation.

Please cite this article in press as: J.H. Park et al., Suppression of threshold voltage variability in MOSFETs by adjustment of ion implantation parameters, Superlattices and Microstructures (2017), https://doi.org/10.1016/j.spmi.2017.10.034