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Performance analysis of asymmetric dielectric modulated dual short gate tunnel field effect transistor

Adhithan Pon, A. Santhia Carmel, A. Bhattacharyya, R. Ramesh*

Device Modeling Lab, School of Electrical & Electronics Engineering, SASTRA University, Thanjavur, India

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ABSTRACT

In this work, a novel asymmetric dielectric modulated dual short gate (ADMDG) TFET is designed and their performance was analysed. The ADMDG TFET using silicon, germanium, and SiGe as channel and source materials were simulated and results are compared with conventional DGTFET. The device simulation has been performed using Sentaurus TCAD simulator. It is found that the proposed structure provides overall improved performance for silicon TFET such as higher on-current (I_{on} = 4.2 μA), smaller SS = 40mV/decade and maximum I_{on}/I_{off} ratio (8.2×10^{10}) compared to conventional DGTFET. The on-current values obtained for SiGe source, Ge source and Ge channel ADMDG TFET are 0.22 mA, 0.69 mA and 0.14 mA respectively compared to silicon ADMDG TFET but compromises other dc parameters such as SS and I_{on}/I_{off} ratio. For CMOS circuits, the p-type silicon TFET of the proposed structure were also simulated and presented. Moreover, the proposed TFET structure is also simulated for different temperatures and its performance were compared and analysed.

1. Introduction

Tunnel Field Effect Transistor (TFET) is a favorable device that offers lower leakage current and subthreshold swing (SS) and has the ability to operate at the very low supply voltage. It acquires band-to-band tunneling (BTBT) process for the flow of carriers unlike traditional MOSFETs as they use thermionic emission over the barrier [1]. Additionally, the fabrication techniques for TFET is compatible with the existing CMOS fabrication flow, it is highly immune to SCEs due to inter band tunneling. TFETs are ambipolar in nature and their on-currents are smaller than the MOSFETs hence the TFET switching speed is smaller [2]. The ambipolarity of TFET can be subdued, but the solution increases the complexity of device fabrication. To suppress the ambipolarity in gate all around TFET (GAA-TFET), gate engineering has been included [3]. The implementation of dielectric engineering increases the on-current of the device [4]. A double gate Tunnel Field effect transistor (DG-TFET) with a Gate Stack (GS) design has been reported [5]. The drive current in a DG-TFET can be enhanced with an asymmetric gate oxide and source pocket [6].

Short gate TFETs with underlap are also suggested to subdue the ambipolar behavior and to elevate the switching speed [7]. It has been reported that the tunneling current can be increased by minimizing the gate oxide thickness or by using high-k dielectrics [8]. The advantage of using a high-κ material in a TFET is that a low equivalent oxide thickness can be obtained

* Corresponding author.
E-mail address: ramesh24.dr@gmail.com (R. Ramesh).

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without decreasing the physical thickness of the gate, thus avoiding the problem of direct tunneling of the carriers through the gate oxide [9].

In TFETs, the tunneling area is present in the channel region interface near the source side. The implementation of multiple gate structure in TFETs increases the effective tunneling area, leads to superior gate control over the channel potential and increases the I_{on} values. This behavior increases both the ambipolar current and I_{off} values. To minimize the ambipolarity and the I_{off} values in the TFET, asymmetrical gate structures have been proposed. The implementation of the symmetric gate structure in TFETs increase the band-to-band tunneling (BTBT) on the source and drain sides. In an asymmetrical gate design, the properties of the gate on the source and the drain sides are different. The introduction of HfO_2 gate oxide at the source side and SiO_2 at the drain side induces local minima at the edge of the conduction band at the tunneling junction (source-channel) which improves the subthreshold swing and enhances the I_{on}. The length of the high-κ gate needs to be optimized for improved device performance [8]. A short gate TFET operating at a supply voltage less than 0.5 V for low-power digital applications has also been investigated [10]. The inclusion of pocket doping in the TFET donates another electric field component to the intrinsic region and improves the tunneling current of the device. This phenomenon further reduces the subthreshold slope values [11]. The electrical properties of TFET made of silicon or germanium exhibit indirect BTBT, while compound materials (InAs, SiGe) show direct BTBT phenomena.

In this paper, an asymmetric short gate TFET architecture with gate engineering is studied and its performance is analysed. Different types of asymmetric TFET structures such as silicon TFET, silicon channel-germanium (Ge) source, silicon source-Ge channel, silicon source-SiGe (silicon-germanium) channel, SiGe source-silicon channel and SiGe source with n^+ pocket-silicon channel were constructed and their performance were compared and studied.

2. Device modeling and simulation

Fig. 1 shows the proposed asymmetric TFET structure with device dimensions. The comprehensive length of the device is 100 nm. The upper gate length ($L_g = L_1+L_2$) is 32 nm having $L_1 = 16$ nm and $L_2 = 16$ nm. The lower gate length (L_{gl}) is 21 nm. The silicon film thickness (t_{si}) is 10 nm, oxide thickness (t_{ox}) is 2 nm and pocket width is 2 nm. The gate work function for the

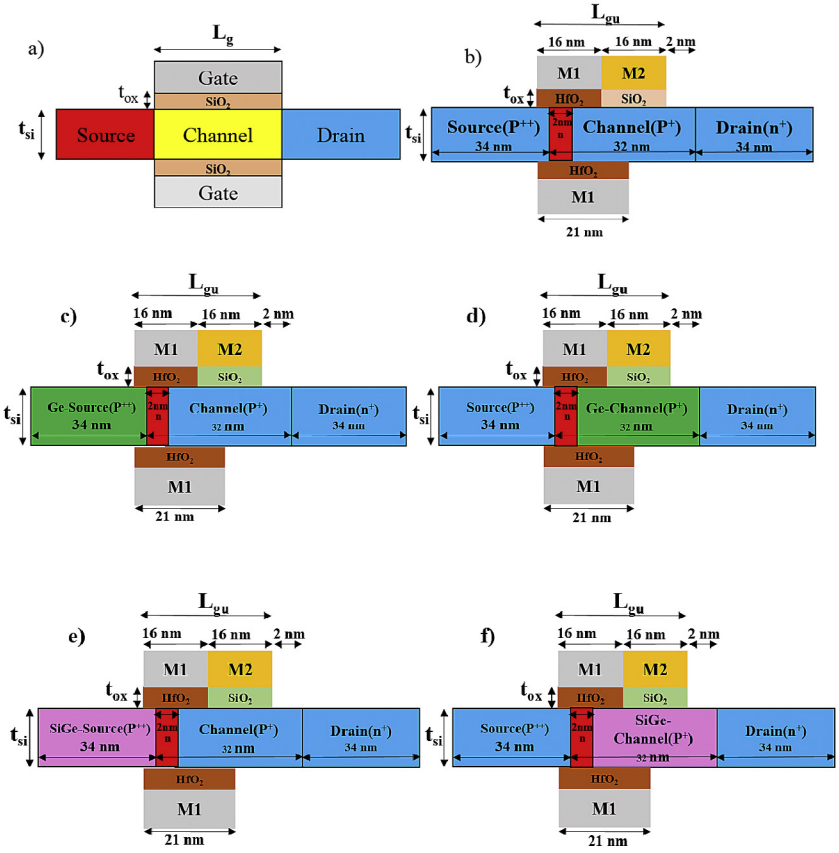

Fig. 1. Different structures of DG TFET a) Conventional DG TFET b) ADMDG silicon TFET c) ADMDG Ge source-silicon channel TFET d) silicon source-Ge channel ADMDG TFET e) SiGe source-silicon channel ADMDG TFET f) silicon source SiGe channel ADMDG TFET.