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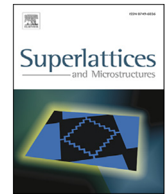

Current switching ratio optimization using dual pocket doping engineering

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This paper presents a smart idea to maximize current switching ratio of cylindrical gate tunnel FET (CGT) by growing pocket layers in both source and channel region. The pocket layers positioned in the source and channel of the device provides significant improvement in ON-state and OFF-state current respectively. The dual pocket doped cylindrical gate TFET (DP-CGT) exhibits much superior performance in term of drain current, transconductance and current ratio as compared to conventional CGT, channel pocket doped CGT (CP-CGT) and source pocket doped CGT (SP-CGT). Further, the current ratio has been optimized w.r.t. width and instantaneous position both the pocket layers. The much improved current ratio and low power consumption makes the proposed device suitable for low-power and high speed application. The simulation work of DP-CGT is done using 3D Sentaurus TCAD device simulator from Synopsys.

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1. Introduction

In the present times, the traditional complementary metal oxide semiconductor (CMOS) technology suffers from two major setbacks of finding difficulty in reducing the supply voltage and keeping the rising OFF-state leakage current within limit [1,2]. This also leads to increase in subthreshold swing (SS) which is undesirable in low-power application. Tunnel field-effect transistor (TFET) is the one of the emerging device which is capable of reducing supply voltage and providing SS below 60 mV/decade due to its inter-band tunneling mechanism [3–8]. Also it reduces short channel effects and leakage current significantly for small dimension as the current characteristics is insensitive to gate length [1]. Thus, a number of TFET models using single gate, double gate and cylindrical gate structures have been developed recently to maximize the device performance and scaling capability [3–11]. Among all, cylindrical gate TFET provides much improved analog performance because of its typical natural length and channel confinement [8–11]. Like other TFET structures, cylindrical gate TFET (CGT) also exhibits low ON-state current as compared to conventional MOSFETs, thus leads to degradation in current switching ratio (I_{ON}/I_{OFF}). The low current ratio is one of the important setbacks in low-power application as it increases static power consumption. The current ratio needs to be maximized as much as possible to reduce the requirement of supply voltage for small-scale transistors. So, the need of the hour is to design a smart strategy which could provide high ON-state current without degrading OFF-state leakage current. In recent times, many researchers have proposed several techniques such as band-gap modulation [12], hetero-junction mechanism [13–16], pocket doping engineering [17–20], etc., to enhance the current performance of the device.

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The introduction of highly doped pocket layer in the source leads to improve in I_{ON}/I_{OFF} ratio by increasing ON-state current significantly [19,20]. This is as a result of high electric field at the tunneling junction. Similarly the current ratio increases considerably with the pocket layer positioned in the channel as it reduces OFF-state current substantially. Thus the idea is to propose a smart strategy which will maximize the current ratio by considering the advantages of both types of pocket engineering. In this work, we have developed pocket layers in both the source and channel of cylindrical gate TFET to achieve an optimum ON-state current without affecting OFF-state current. The pocket doping epitaxial structure can be experimentally fabricated using Molecular Beam Epitaxy (MBE) and Metal Organic Vapor Phase Epitaxy (MOVPE) techniques [21,22]. The dual pocket doped cylindrical gate TFET (DP-CGT) exhibits higher drain current, greater transconductance and much superior I_{ON}/I_{OFF} ratio as compared to conventional CGT, channel pocket doped CGT (CP-CGT) and source pocket doped CGT (SP-CGT). The current ratio is further optimized with the variation of position, width and doping concentration of both the pocket layers. Thus, DP-CGT can be an evolving device to replace MOS technology due to its much reduced power consumption and higher current ratio. The extensive simulation of the proposed DP-CGT device has been carried out using Synopsys TCAD device simulator [23].

2. Device structure and simulation setup

Fig. 1a–c illustrate the cross-sectional view of CGT, CP-CGT and SP-CGT models respectively. The cross-sectional view of the proposed Dual Pocket doped Cylindrical Gate TFET (DP-CGT) is shown in Fig. 1d. The proposed model is developed with channel length (L_c) of 50 nm and source/drain length (L_s/L_d) of 20 nm respectively. The source (p+), channel (p) and drain (n+) regions of the present device are doped with impurity concentration of $N_S = 5 \times 10^{19}\ cm^{-3}$, $N_C = 10^{15}\ cm^{-3}$ and $N_D = 10^{19}\ cm^{-3}$. The drain is doped lightly as compared to source in order to reduce the ambipolar effect and OFF-state current [24]. Here two pocket regions (P1 and P2) are introduced in the source and channel correspondingly. The P1 pocket layer (p++) is developed in the source region at a distance of $L_{P1} = 0.5\ nm$ from the tunneling junction with doping concentration of $N_{P1} = 10^{21}\ cm^{-3}$. The 2nd pocket layer P2 is doped with pentavalent impurity of $N_{P2} = 10^{19}\ cm^{-3}$ and is positioned in the channel region adjacent to the interface ($L_{P2} = 0\ nm$). The width of the two pocket layers (W_{P1} and W_{P2}) are considered to be 1 nm each. However, the position and width of the pocket regions are optimized to achieve the maximum current switching ratio (I_{ON}/I_{OFF}). The radius ($t_{si}/2$) and gate oxide thickness (t_{ox}) of the cylindrical TFET structure is 5 nm and 2 nm respectively. The work-function of the gate metal is considered as 4.2 eV.

The presence of pocket doping in the channel of CGT decreases OFF-state leakage current significantly, thus improves current switching ratio. This reduces subthreshold swing further and makes it suitable for low-power application. Similarly the ON-state current increases considerably with the introduction of highly doped pocket layer which is due to high

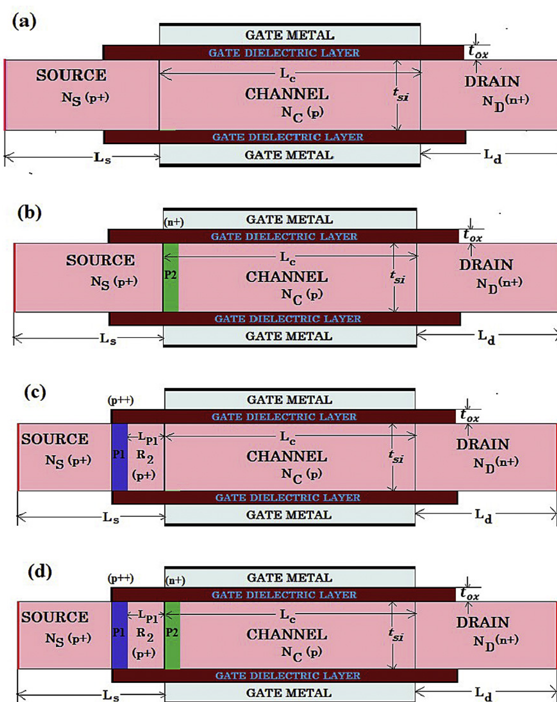

Fig. 1. Schematic cross-sectional view of n-channel (a) conventional cylindrical gate TFET (CGT) (b) channel pocket doped CGT (CP-CGT) (c) source pocket doped CGT (SP-CGT) (b) dual pocket doped CGT (DP-CGT).

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