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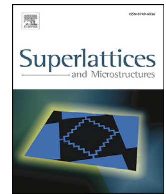

Charge plasma based source/drain engineered Schottky Barrier MOSFET: Ambipolar suppression and improvement of the RF performance

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ABSTRACT

This paper reports a novel device structure for charge plasma based Schottky Barrier (SB) MOSFET on ultrathin SOI to suppress the ambipolar leakage current and improvement of the radio frequency (RF) performance. In the proposed device, we employ dual material for the source and drain formation. Therefore, source/drain is divided into two parts as main source/drain and source/drain extension. Erbium silicide ($ErSi_{1.7}$) is used as main source/drain material and Hafnium metal is used as source/drain extension material. The source extension induces the electron plasma in the ultrathin SOI body resulting reduction of SB width at the source side. Similarly, drain extension also induces the electron plasma at the drain side. This significantly increases the SB width due to increased depletion at the drain end. As a result, the ambipolar leakage current can be suppressed. In addition, drain extension also reduces the parasitic capacitances of the proposed device to improve the RF performance. The optimization of length and work function of metal used in the drain extension is performed to achieve improvement in device performance. Moreover, the proposed device makes fabrication simpler, requires low thermal budget and free from random dopant fluctuations.

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1. Introduction

Due to its simpler fabrication and low thermal budget requirement, SB MOSFET has been regarded as a potential alternative to replace conventional MOSFET for future nanoscale Integrated Circuits [1–8]. It is well known that continued downscaling arises several issues such as increased source/drain (S/D) parasitic resistances, fabrication complexity and severe short channel effects [9,10]. To solve the aforementioned issues, SB MOSFET has been extensively studied by various research groups in the past decade. It offers low parasitic S/D resistances, simpler fabrication and increased immunity to short channel effects. In addition, it has atomically abrupt junctions, superior scalability, and free from random dopant fluctuations (RDF) [11]. Irrespective of their numerous advantages, it suffers from low drive current due to presence of intrinsic Schottky barrier between metal S/D and semiconductor. To improve the drive current of the conventional SB MOSFET highly doped dopant

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segregated layers (DSL) have been used [12,13]. This DSL significantly modulates the SB height and width to improve the drive current of the device [14,15]. However, introducing dopants to form dopant segregated (DS) SB MOSFET results in fabrication complexity, random dopant fluctuations and increased thermal budget [16]. To solve the problem associated with the DS SB MOSFET, recently novel device structure is proposed and studied named as Source engineered (SE) SB MOSFET [17]. In this device, charge plasma concept is used to improve the device performance by modifying the SB width. This SE SB MOSFET offers low temperature process, elimination of doping and free from random dopant fluctuations. Apart from these, SE SB MOSFET suffers from ambipolar leakage current even for the negative gate bias and inferior RF performance due to increased parasitic capacitance. To suppress the ambipolar leakage current few methods were reported, which are compared and summarized in Table 1. Furthermore, to enhance the RF performance of the device several works reported i.e., R. Valentin et al. [24] optimized the RF performance of metallic source/drain SOI MOSFETs using dopant segregation at the Schottky interface. M. J. Martin et al. [25,26] investigated RF dynamic and noise performance of metallic Source/Drain SOI n-MOSFETs and performed Monte carlo study of DS SB SOI MOSFETs for enhancement of the RF performance. However, aforementioned works for enhancement of RF performance uses underlap channel architecture at the source and drain end resulting reduction in drive current of the device.

To address the aforementioned issues, we have proposed and investigated a novel device structure named as S/D Engineered SB MOSFET as given in Table 1. In the proposed device, we have employed source and drain extension to modulate the SB width at the source and drain end. The source extension is identical as employed in the SE SB MOSFET. In addition, in the proposed device, drain is divided into two parts as the main drain and the drain extension also made by Hafnium. Due to use of hafnium metal, the undoped SOI region below the drain extension converted into n^+ region by charge plasma concept. This effectively increases the SB width at the drain side in the off-state. As a result, the reduction in ambipolar current can be obtained for negative gate bias condition. In addition, drain extension also improves the RF performance of the device by reducing parasitic capacitances. Moreover, the length and work function of the metal used to form the drain extension is successfully optimized to effective control of ambipolar leakage current with improvement in RF performance without affecting the drive current of the device. The proposed device makes fabrication simpler, requires low thermal budget and free from random dopant fluctuations (RDF).

2. Device structure and simulation methodology

2.1. Device structure

The schematic views of the conventional SE SB MOSFET and the proposed S/D Engineered SB MOSFET is shown in Fig. 1(a) and (b), respectively. The following are the common simulation parameters for above mentioned device structures: SOI thickness (T_{si}) = 10 nm, gate oxide thickness (T_{ox1}) = 2 nm, bottom oxide thickness of 10 nm, gate work function of 4.65 eV and for the main S/D formation, $ErSi_{1.7}$ having work function of 4.45 eV is employed. To form source and drain extension hafnium metal having work function of 3.8 eV is employed. However, the drain extension is only employed in the proposed device. The oxide thickness below the extended source and extended drain (T_{ox2}) is 0.2 nm. The spacing of source to gate (L_{gs}) of conventional SE SB MOSFET is 5 nm. However, the spacing between source to gate (L_{gs}) and drain to gate (L_{gd}) is same as 5 nm for the proposed device. For maintaining induced carrier distribution uniform beneath the source and drain extension, SOI thickness has to be kept within the Debye length, that is

Table 1
Comparison of the present work with previously reported work based on ambipolar leakage reduction.

References	Methods	Salient features	Disadvantages
[18]	inserted insulator such as LiF and Si_3N_4 between the metal S/D and semiconductor	depin the fermi level, efficient suppression of ambipolar behaviour	increased fabrication complexity, tradeoff between maximum on-current, suppression of leakage current, and contact length
[19,20]	used field-induced drain extension between the drain and channel interface	all dopings are eliminated	increased fabrication complexity, suffers from severe short channel effects for n-channel operation, required two different gates such as main gate and sub gate
[21]	employed recessed channel architecture with asymmetric S/D contacts	insensitive to the feature size variations, effectively suppressed short-channel effects	ambipolar leakage was not fully suppressed, required asymmetric S/D contacts
[22]	used underlap gate at the drain end	simpler fabrication, exhibit six to seven decade reduction in ambipolar leakage	reduced drive current, suffers from random dopant fluctuations
[23]	used asymmetric isolated gate structure	effectively suppressed ambipolar leakage	increased fabrication complexity, suffers from random dopant fluctuations, required two different work function metal gates
Present Work	using drain extension to modulate the SB width at the drain end	eliminating the need of doping, requires low thermal budget, simpler fabrication, free from random dopant fluctuations, improves RF performance, improves drive current, effectively suppressed ambipolar leakage	limited tunability, pitch scalability, required dual material for S/D formation

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