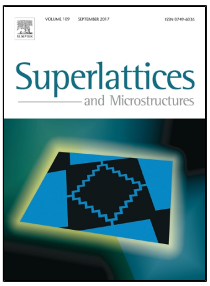
Accepted Manuscript



An ultra-low specific on-resistance double-gate trench SOI LDMOS with P/N pillars

Dong Yang, Shengdong Hu, Jianmei Lei, Ye Huang, Qi Yuan, Yuyu Jiang, Jingwei Guo, Kun Cheng, Zhi Lin, Xichuan Zhou, Fang Tang

PII:	S0749-6036(17)31910-9
DOI:	10.1016/j.spmi.2017.09.033
Reference:	YSPMI 5269
To appear in:	*Superlattices and Microstructures*
Received Date:	11 August 2017
Revised Date:	13 September 2017
Accepted Date:	13 September 2017

Please cite this article as: Dong Yang, Shengdong Hu, Jianmei Lei, Ye Huang, Qi Yuan, Yuyu Jiang, Jingwei Guo, Kun Cheng, Zhi Lin, Xichuan Zhou, Fang Tang, An ultra-low specific on-resistance double-gate trench SOI LDMOS with P/N pillars, *Superlattices and Microstructures* (2017), doi: 10.1016/j.spmi.2017.09.033

Highlights

1. An ultra-low specific on-resistance double-gate trench SOI LDMOS is proposed.
2. The influences of structure parameters on the performances are investigated.
3. A $R_{on,sp}$ of 0.58 mΩ·cm^2 and a figure-of-merit of 62.9 MW/cm^2 are obtained.
4. Figure-of-merit of the proposed structure is enhanced by 308.4%.
5. A significantly optimized dependence of $R_{on,sp}$ on BV is obtained.