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An ultra-low specific on-resistance double-gate trench SOI LDMOS with P/N pillars

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Highlights

1. An ultra-low specific on-resistance double-gate trench SOI LDMOS is proposed.
2. The influences of structure parameters on the performances are investigated.
3. A $R_{on,sp}$ of $0.58 \text{ m}\Omega\cdot\text{cm}^2$ and a figure-of-merit of 62.9 MW/cm^2 are obtained.
4. Figure-of-merit of the proposed structure is enhanced by 308.4%.
5. A significantly optimized dependence of $R_{on,sp}$ on BV is obtained.

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